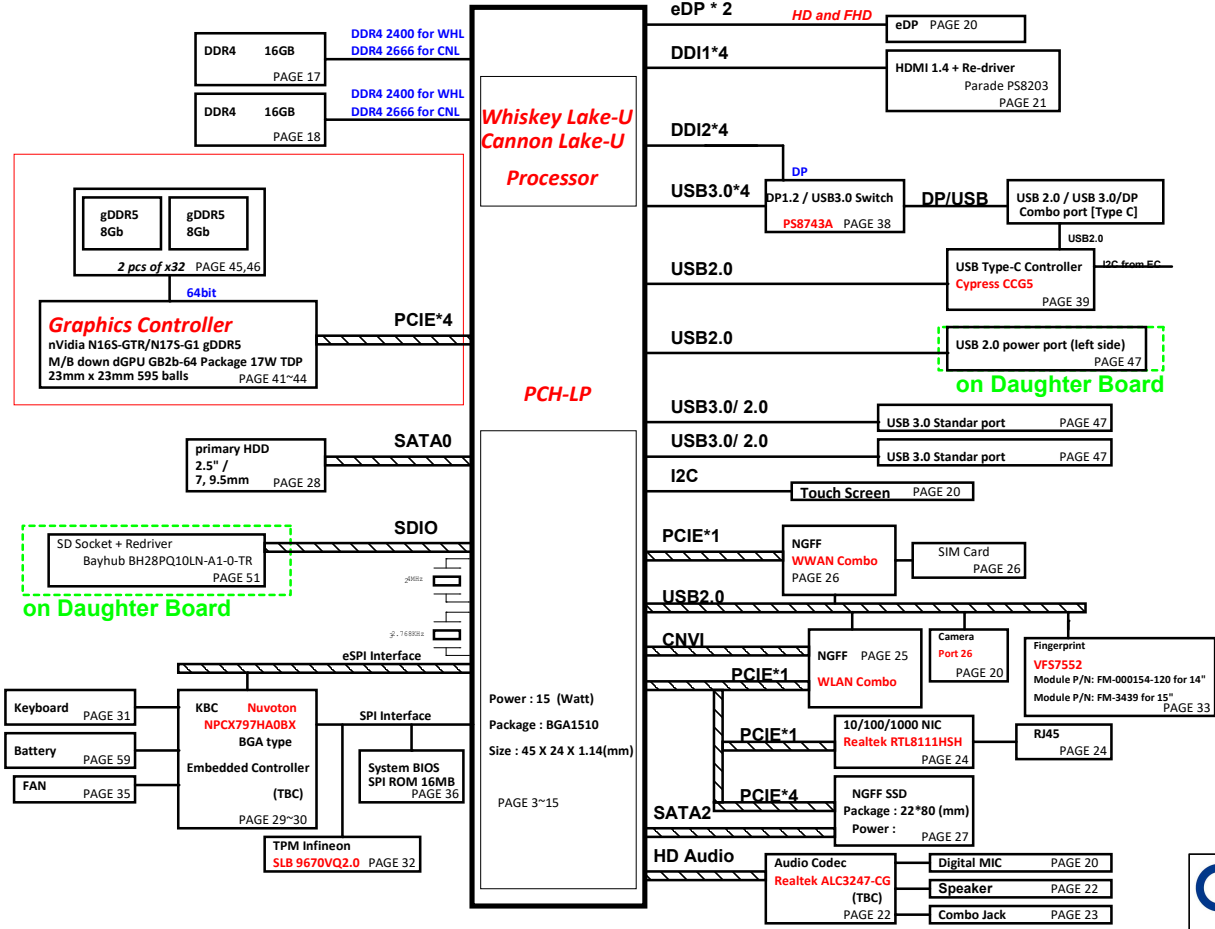
S400 14"/ 15.6" WHL/CNL (UMA/DIS) Block Diagram

01



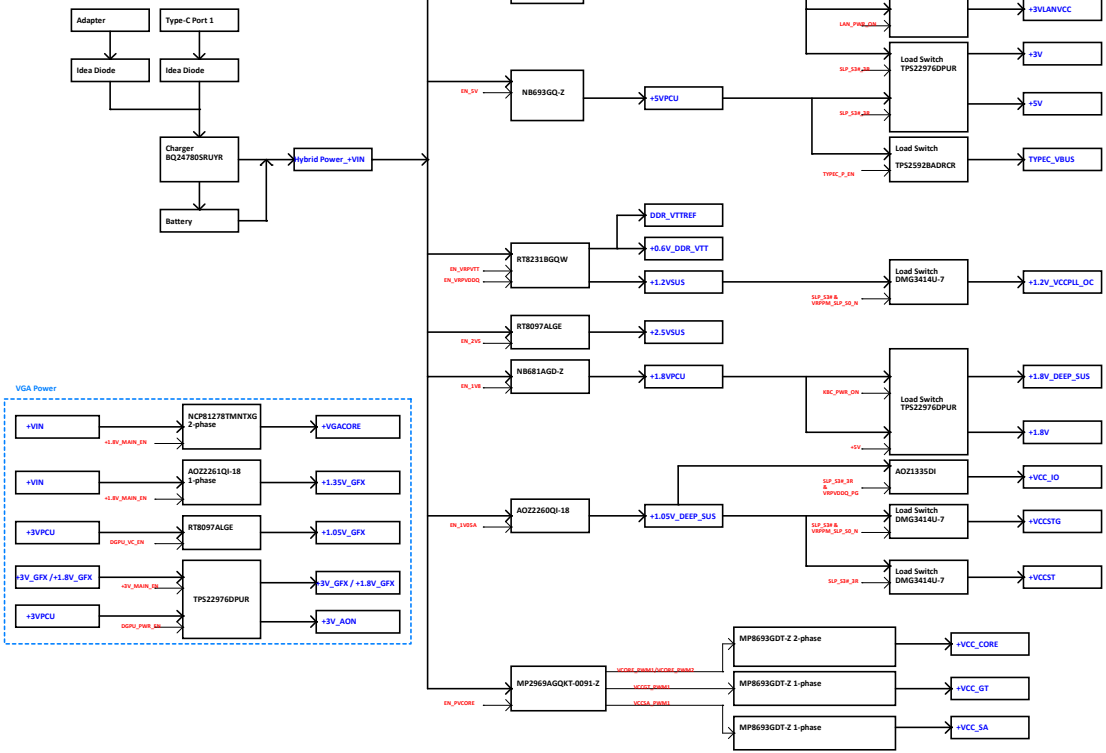
PCB 8L STACK UP (1.1mm)

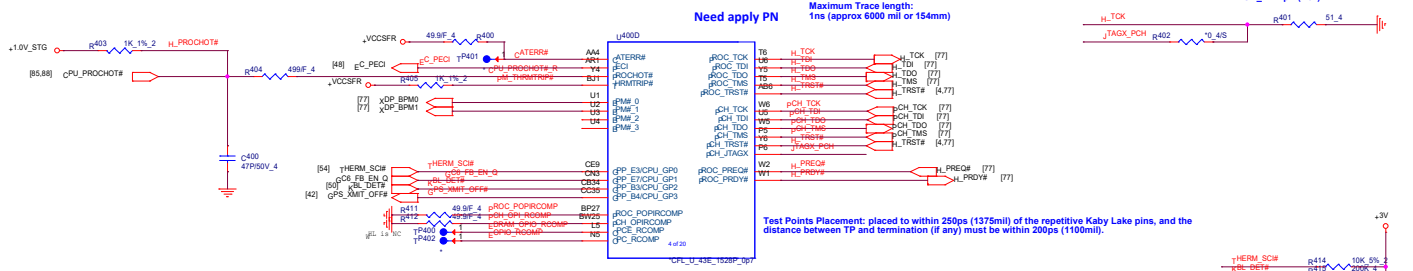
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT

PROJECT :X8B
Quanta Computer Inc.

Size: Custom | Document Number: Block Diagram | Rev: 3A
Date: Monday, October 29, 2018 | Sheet 1 of 106

POWER BLOCK DIAGRAM

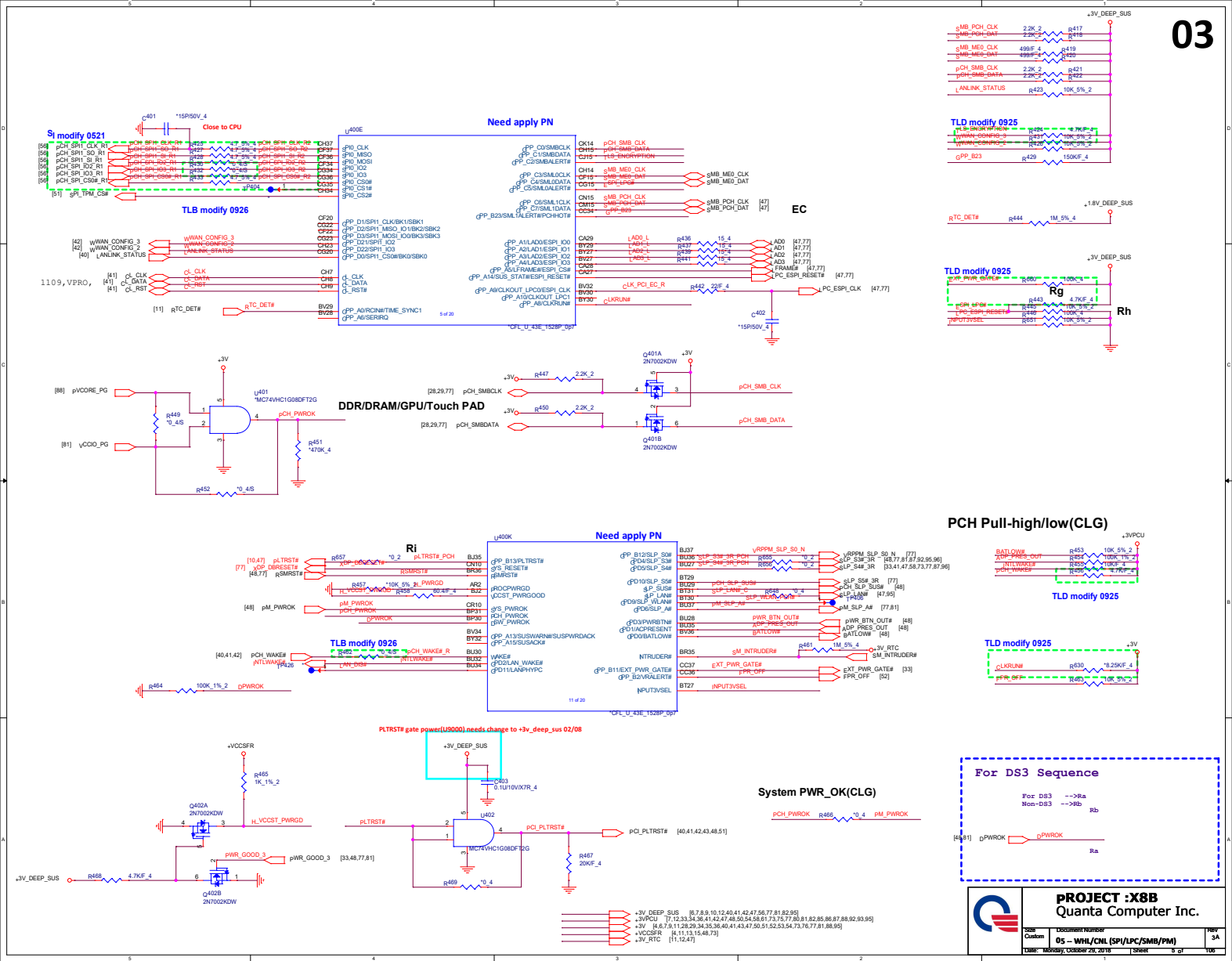




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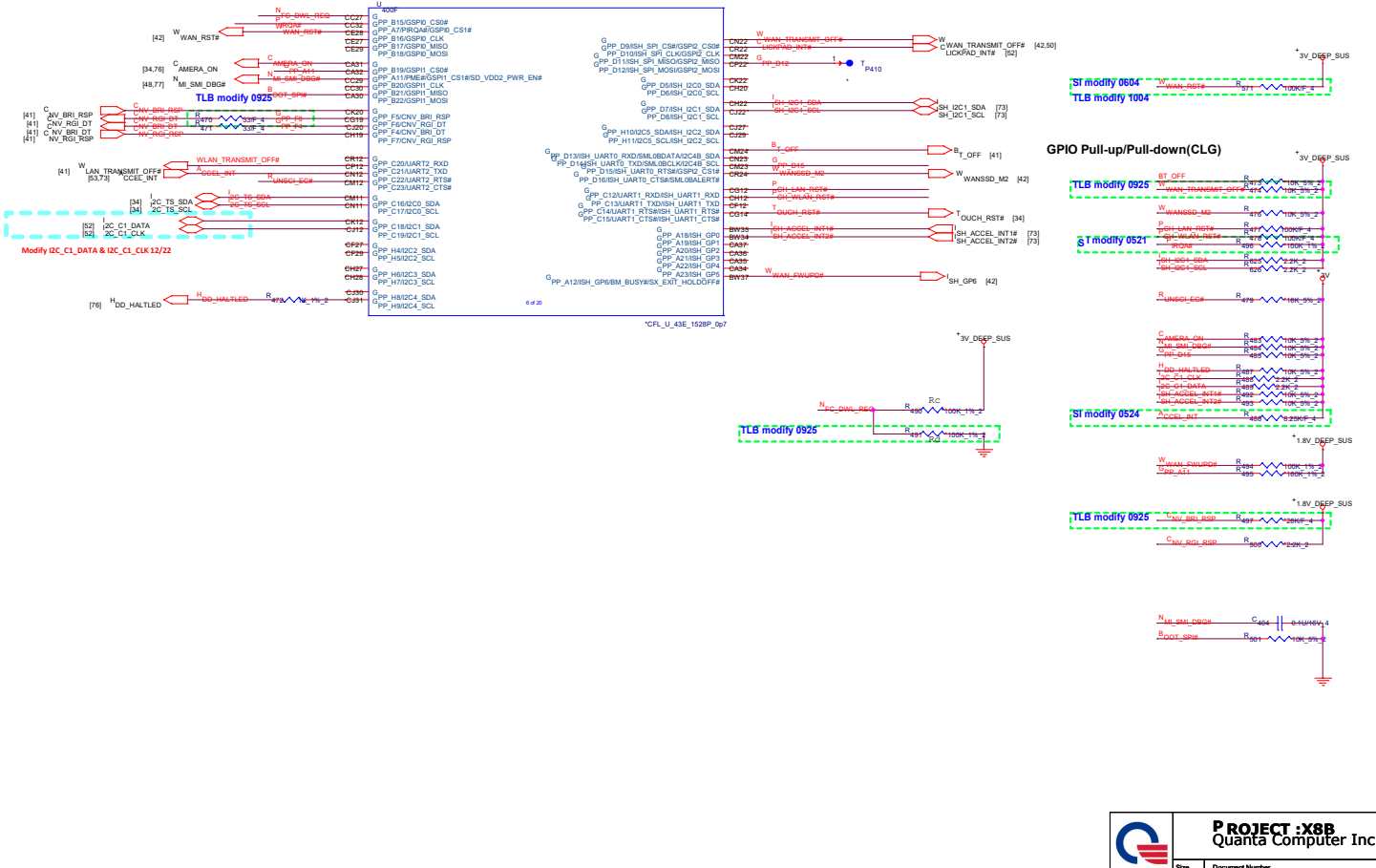
+1.0V_STG [13,15]
+VCCSFR [5,11,13,15,48,73]
+3V [5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95]

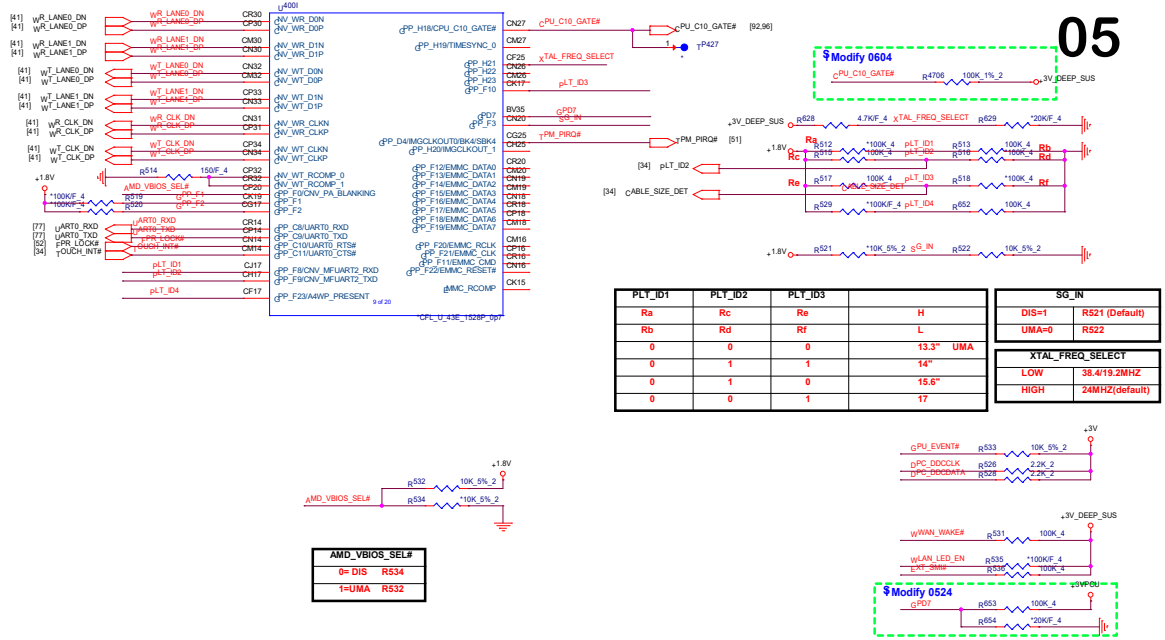
PROJECT :X8B Quanta Computer Inc.			
Size: Custom	Document Number: 04 – WHL/CNL 4/20[MISC/ JTAG]		Rev: 3A
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PROJECT	X8B
	Quanta Computer Inc.
Size	Custom
Document Number	05 – WHL/CNL (SPI/LPC/SMB/PM)
Rev	3A
Date:	Monday, October 29, 2018
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WHL/CNL (GPIO)


TLB modify 0925
Modify I2C_C1_DATA & I2C_C1_CLK 12/22
GPIO Pull-up/Pull-down(CLG)
SI modify 0604
TLB modify 1004
SI modify 0524
SI modify 0521
*CFL_U_43E_1528P_0p7
P PROJECT :X8B
Quanta Computer Inc.
Size Custom
Document Number 06 – WHL/CNL (GPIO)
Rev A
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PLT_ID1	PLT_ID2	PLT_ID3	H
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3" UMA
0	1	1	14"
0	1	0	15.6"
0	0	1	17

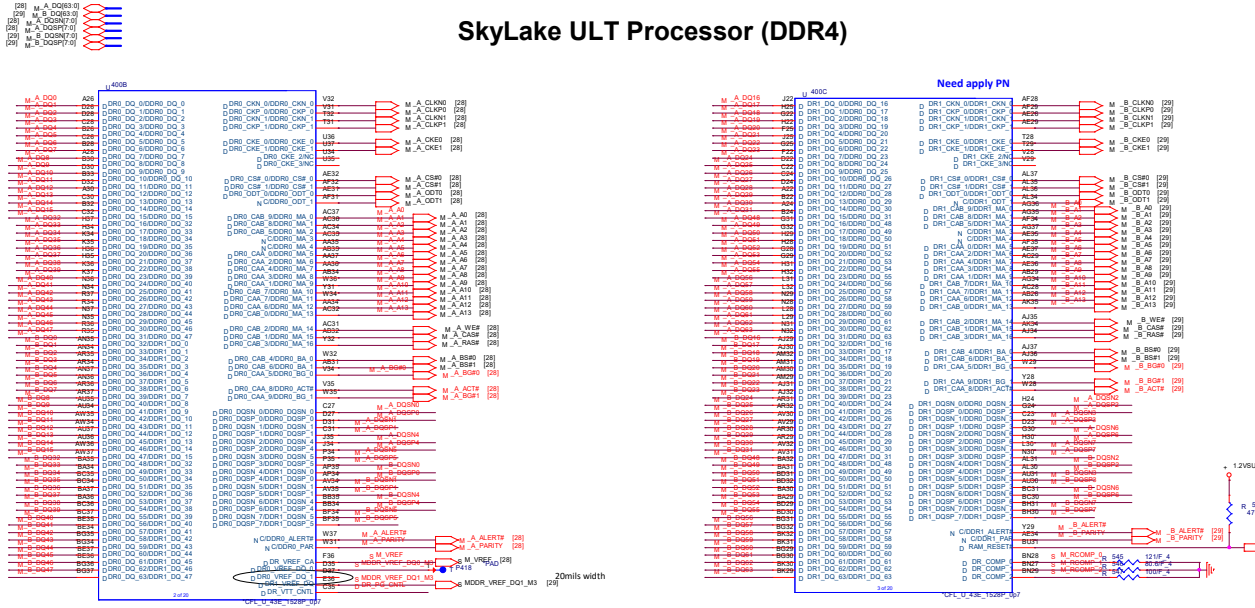
SG_IN	
DIS=1	R521 (Default)
UMA=0	R522

XTAL_FREQ_SELECT	
LOW	38.4/19.2MHZ
HIGH	24MHZ(default)

AMD_VBIOS_SEL#	
0= DIS	R534
1=UMA	R532

R543	WHL	CNL
DISP	24.9ohm	100ohm

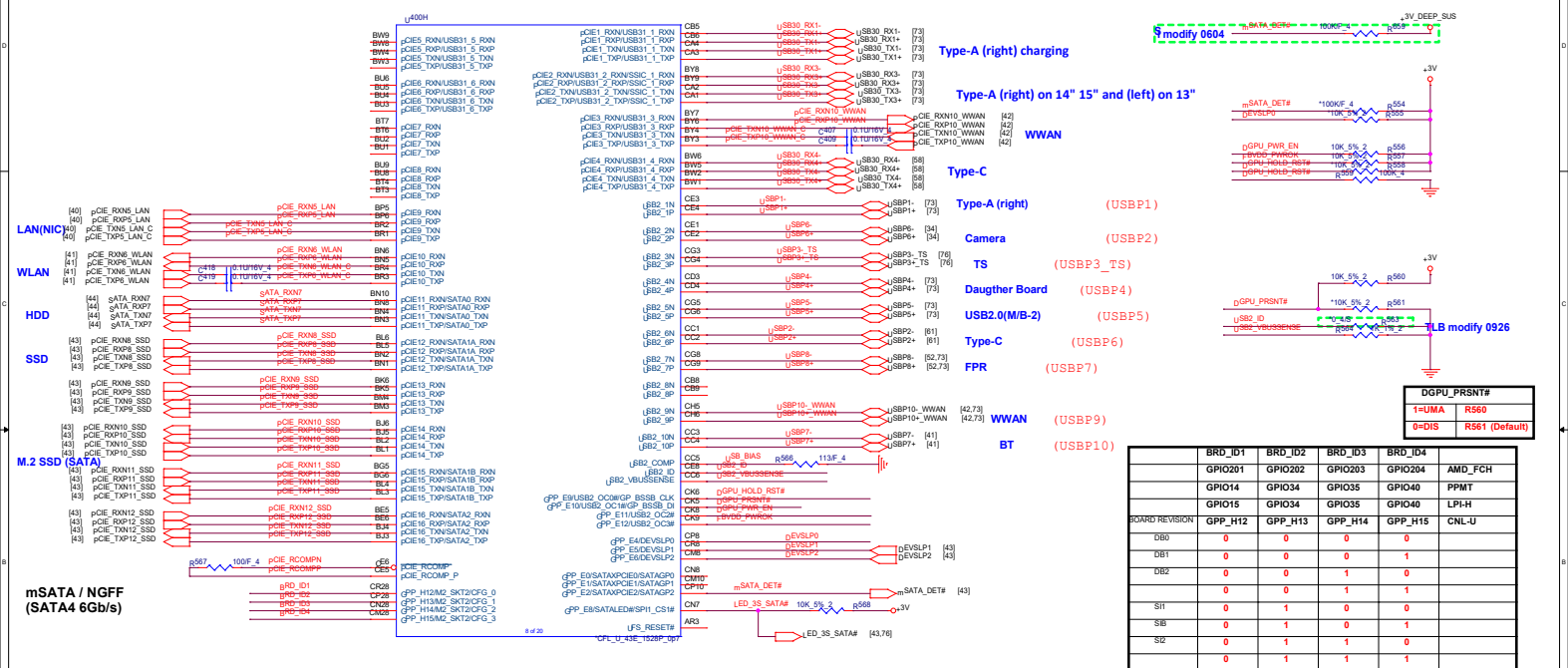
SkyLake ULT Processor (DDR4)



	WHL	CNL
RCOMP0	121ohm	100ohm
RCOMP1	80.6ohm	100ohm
RCOMP2	100ohm	100ohm

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PROJECT :X8B
Quanta Computer Inc.
Size: Custom | Document Number: @ -- WHL/CNL (DDR3-A/B I/F) | Rev: 3 A
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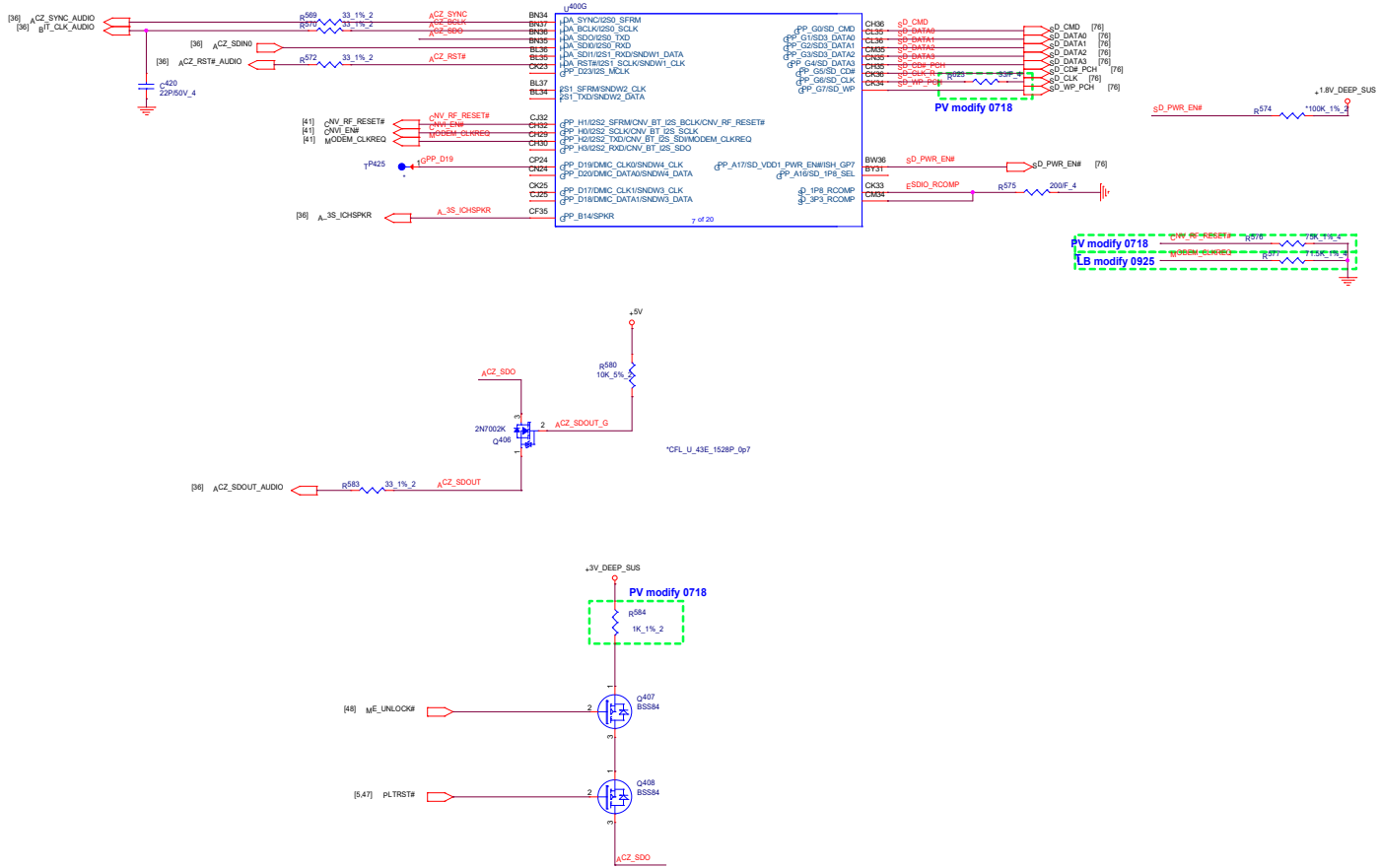
DGPU_PRSNT#	
1=UMA	R560
0=DIS	R561 (Default)

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPP_H12	GPP_H13	GPP_H14	GPP_H15	CNL-U
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
TLB	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	

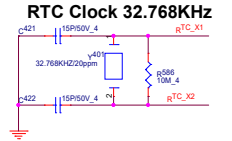
[4,5,6,7,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95] +3V
[5,6,7,8,10,12,40,41,42,47,56,77,81,82,95] 3V_DEEP_SUS

PROJECT :X8B
Quanta Computer Inc.

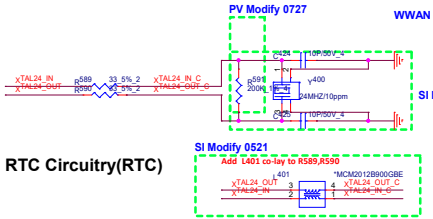
Size	Document Number	Rev
Custom	0g – WHL/CNL (PCIE/USB)	3A
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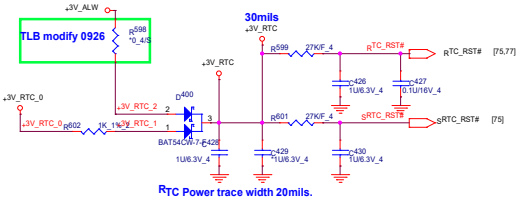

U400G
PV modify 0718
PV modify 0718
LB modify 0925
Q406
2N7002K
Q407
BSS84
Q408
BSS84
*CFL_U_43E_1528P_0p7
PROJECT :X8B
Quanta Computer Inc.
Size: Custom
Document Number: 1g – WHL/CNL (HDA)
Rev: 3A
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RTC Clock 32.768KHz



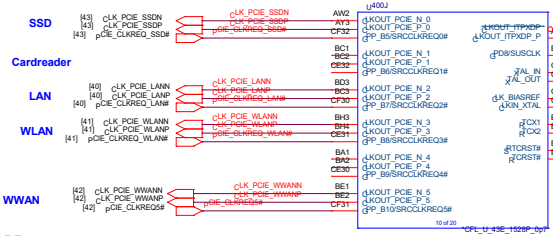
RTC Circuitry(RTC)







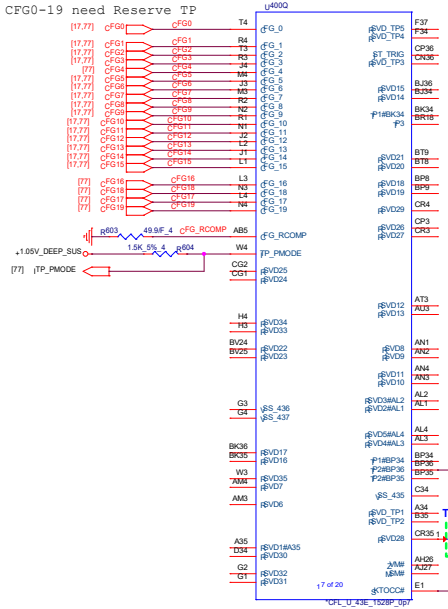
SSD / Cardreader / LAN / WLAN / WWAN



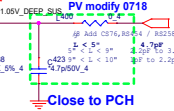
CLK_REQ/Strap Pin(CLG)

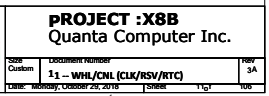


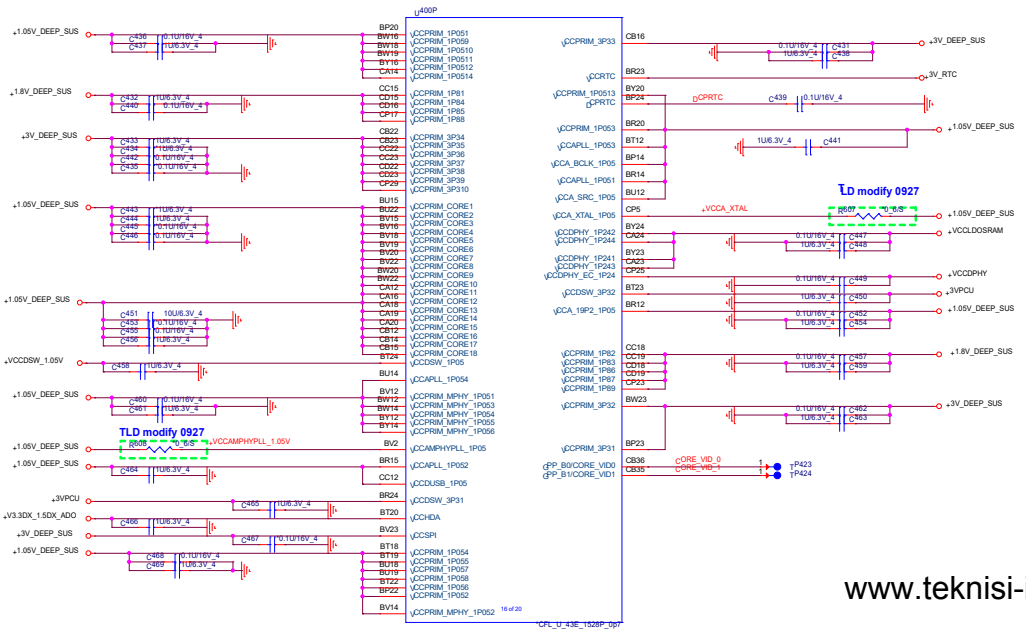
CFG0-19 need Reserve TP

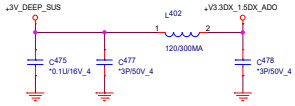


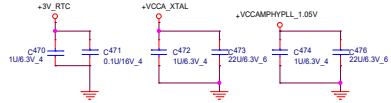
PV modify 0718











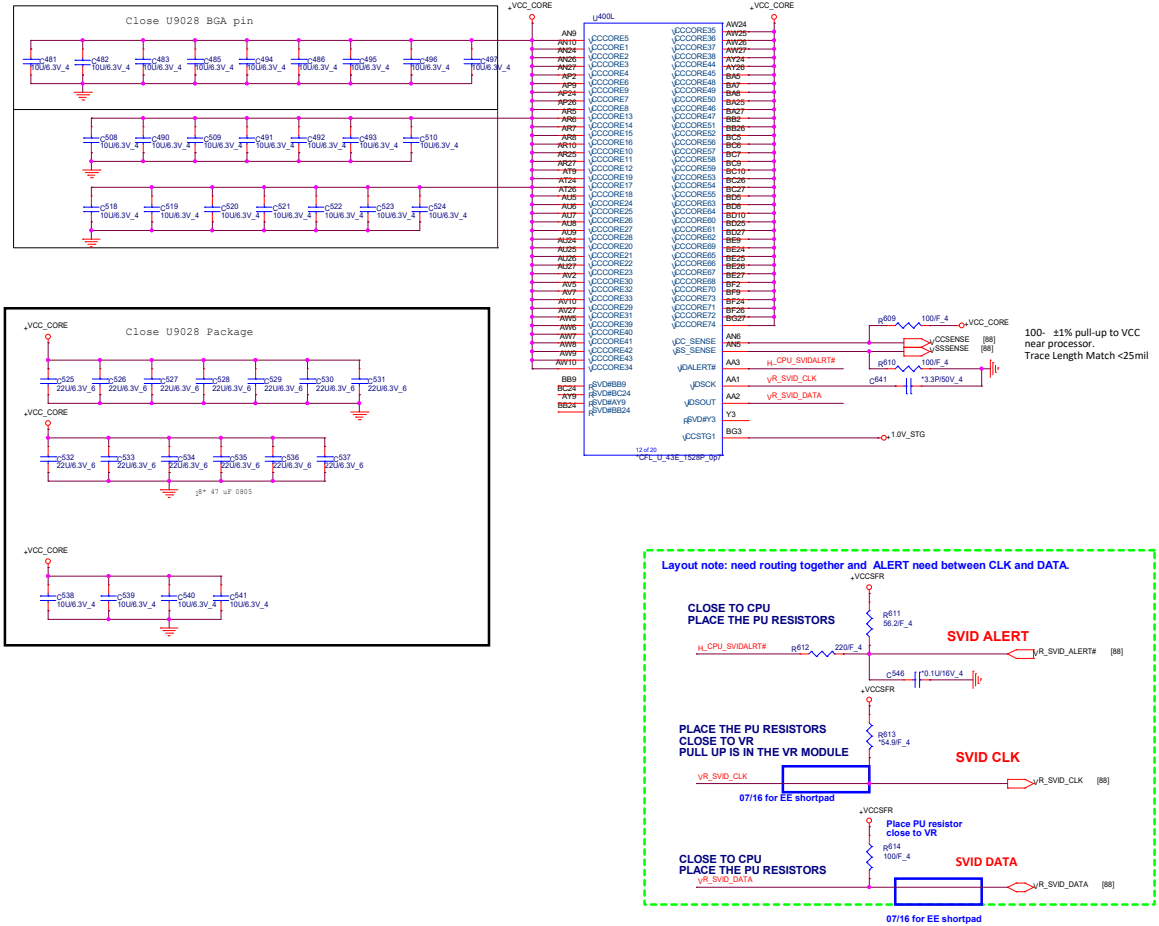
+3V_DEEP_SUS [5,6,7,8,9,10,40,41,42,47,56,77,81,82,95]
+3VPCU [5,7,33,34,36,41,42,47,48,50,54,58,61,73,75,77,80,81,82,85,86,87,88,92,93,95]
+1.05V_DEEP_SUS [11,73,77,92,96]

+3V [4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95]
+1.8V_DEEP_SUS [5,6,10,41,47,81,95]

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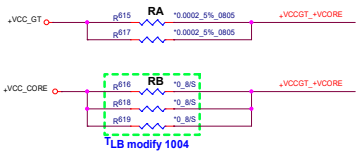
Size	Document Number	Rev
Custom	12 – WHL/CNL (PCH POWER)	3A
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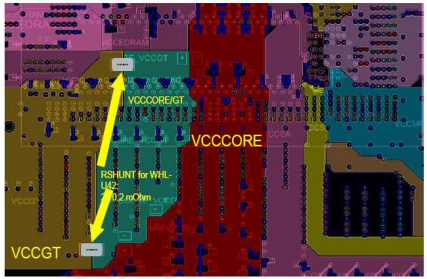
PROJECT :X8B
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Size	Document Number	Rev
Custom	13 – WHL/CNL (POWER-1)	3A
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	WHL-U42f ES1 CNL-U22	WHL-U42 ES2
RA	STUFF	NI
RB	NI	STUFF



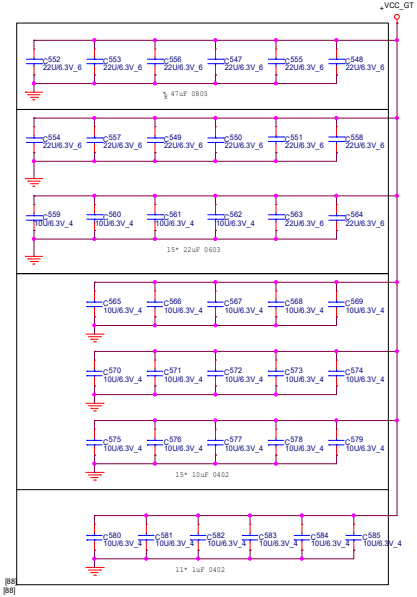
Routing guideline for RSHUNT placement for WHL ES1, CFL43e and CNLU22



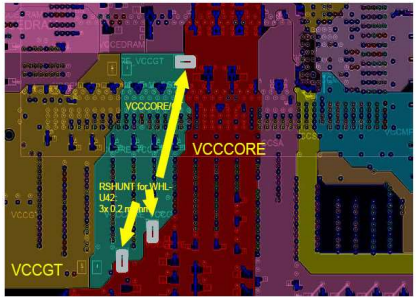
Place 2x 0.2 mOhm RSHUNT for WHL-U42 (ES1)/CFL-U43e/CNL-U22



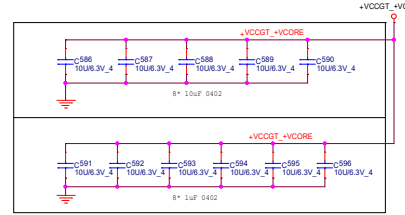
Trace Length Match <25mil



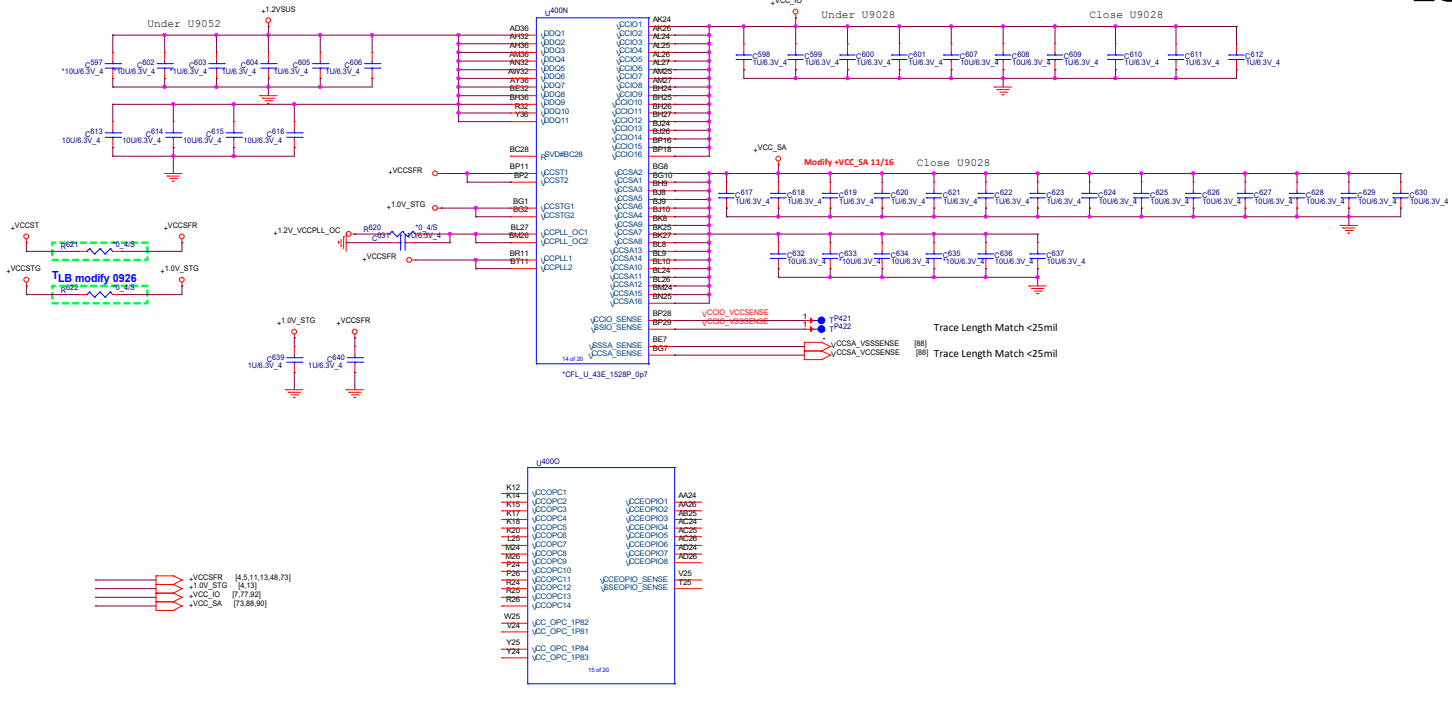
Routing guideline for RSHUNT placement for WHL ES2



Place 3x 0.2 mOhm RSHUNT for WHL-U42 (ES2)



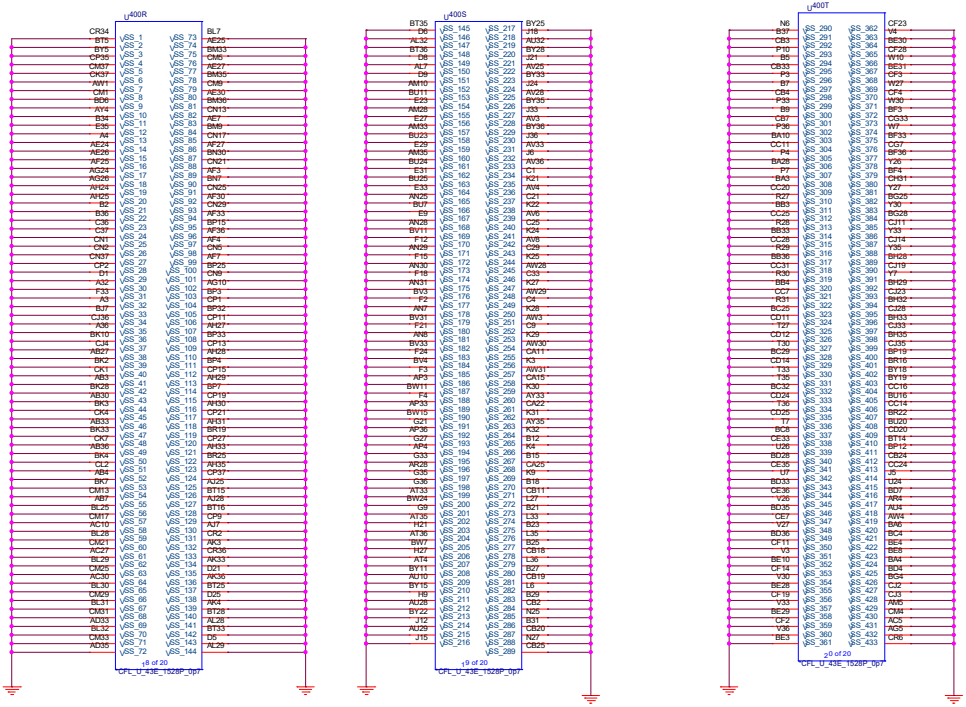
PROJECT :X8B Quanta Computer Inc.			
Size: Custom	Document Number: 14 – WHL/CNL (POWER-2)		Rev: 3A
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pROJECT :X8B

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Size: Custom	Document Number: 15 – WHL/CNL (POWER-3)	Rev: 3A
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Quanta Computer Inc.			
Size: Custom	Document Number: 16 – WHL/CNL (GND)		Rev: 3A
Date: Monday, October 29, 2018	Sheet: 16 of 106		

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

CFG0

1:(DEFAULT) NORMAL OPERATION; NO STALL

0:STALL

PCH/ PCH LESS MODE SELECTION

CFG1

1:(DEFAULT) NORMAL OPERATION

0: PCH-LESS MODE

ALLOW THE USE OF CFG ON LOCKED UNITS

CFG5

1: DISABLED(DEFAULT) - IN THIS CASE, CFG WILL BE ENABLED IN UN-LOCKED UNITS

0: ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG6

1:VRS SUPPORTING SVID PROTOCOL ARE PRESENT

0:NO VR SUPPORTING SVID PROTOCOL ARE PRESENT. THE LINK WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

SAFE MODE BOOT

CFG10 1: POWER FEATURES ACTIVATED DURING RESET

0: POWER FEATURES (ESPECIALLY CLOCK GATING ARE NOT ACTIVATED

PMSYNC ASYNC MODE- PM SYNC

CFG 13 1' - (DEFAULT)SYNCHRONOUS (1 24 MHZ CYCLE PER BIT)

0' - ASYNC - 4-24MHZ CYCLES PER BIT

PM SYNC LEGACY

CFG 12 1' - (DEFAULT) PMSYNC 2.0

0' - LEGACY

DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR ULX-ULT

CFG11 1:(DEFUALT) DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED

0:DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

MODULE NAME	REV	DATE

PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)

CFG3 0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

1 : DISABLED

DISPLAY PORT PRESENCE STRAP

CFG4 0: ENABLED; 1 DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

1: DISABLED; NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2 1: (DEFAULT)NORMAL OPERATION; 0: LANE REVERSAL

PCIE PORT BIFURCATION STRAPS

CFG[6:5] 11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED

10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED

01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED

00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

PEG DEFER TRAINING

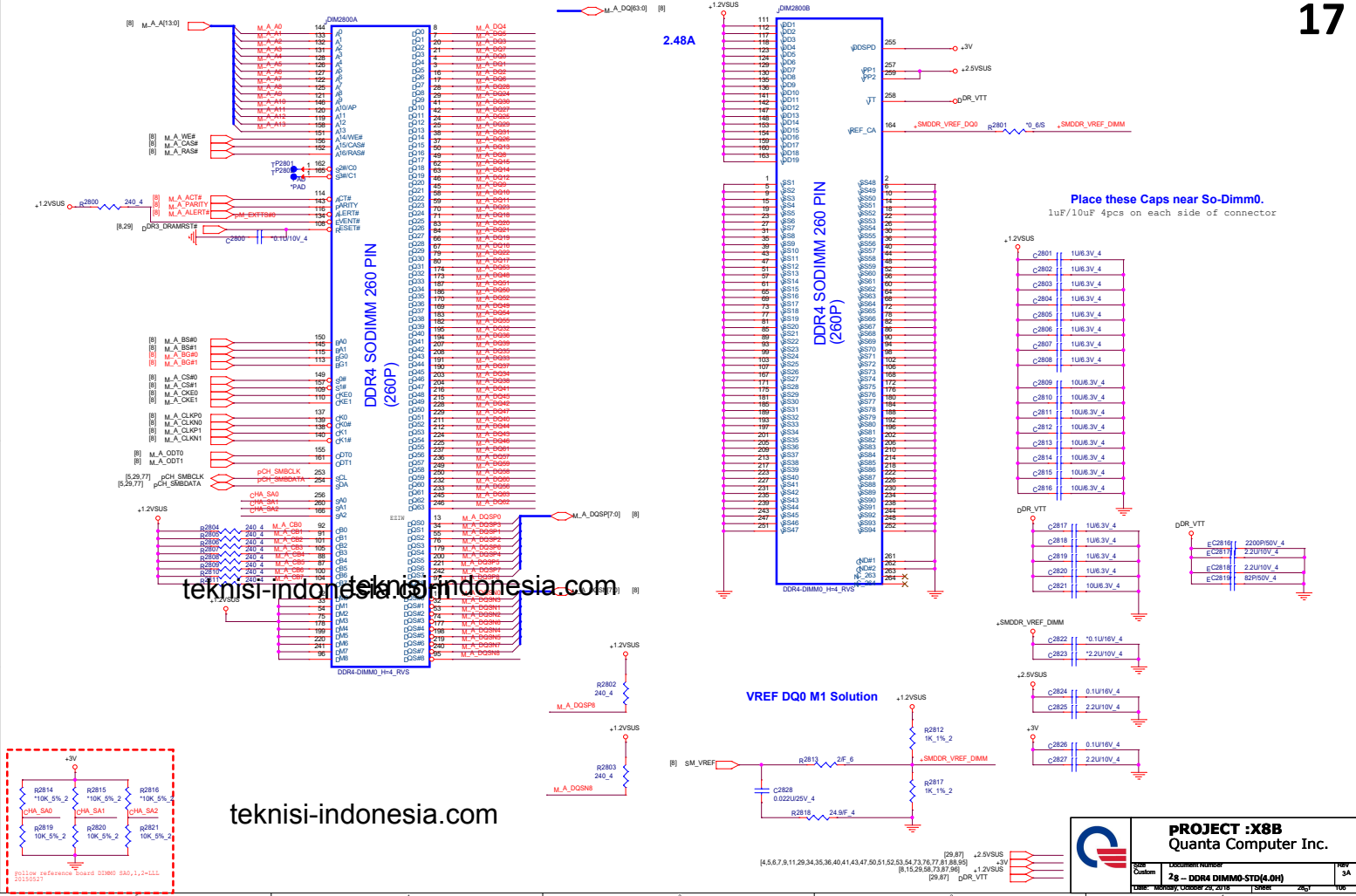
CFG7 1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION

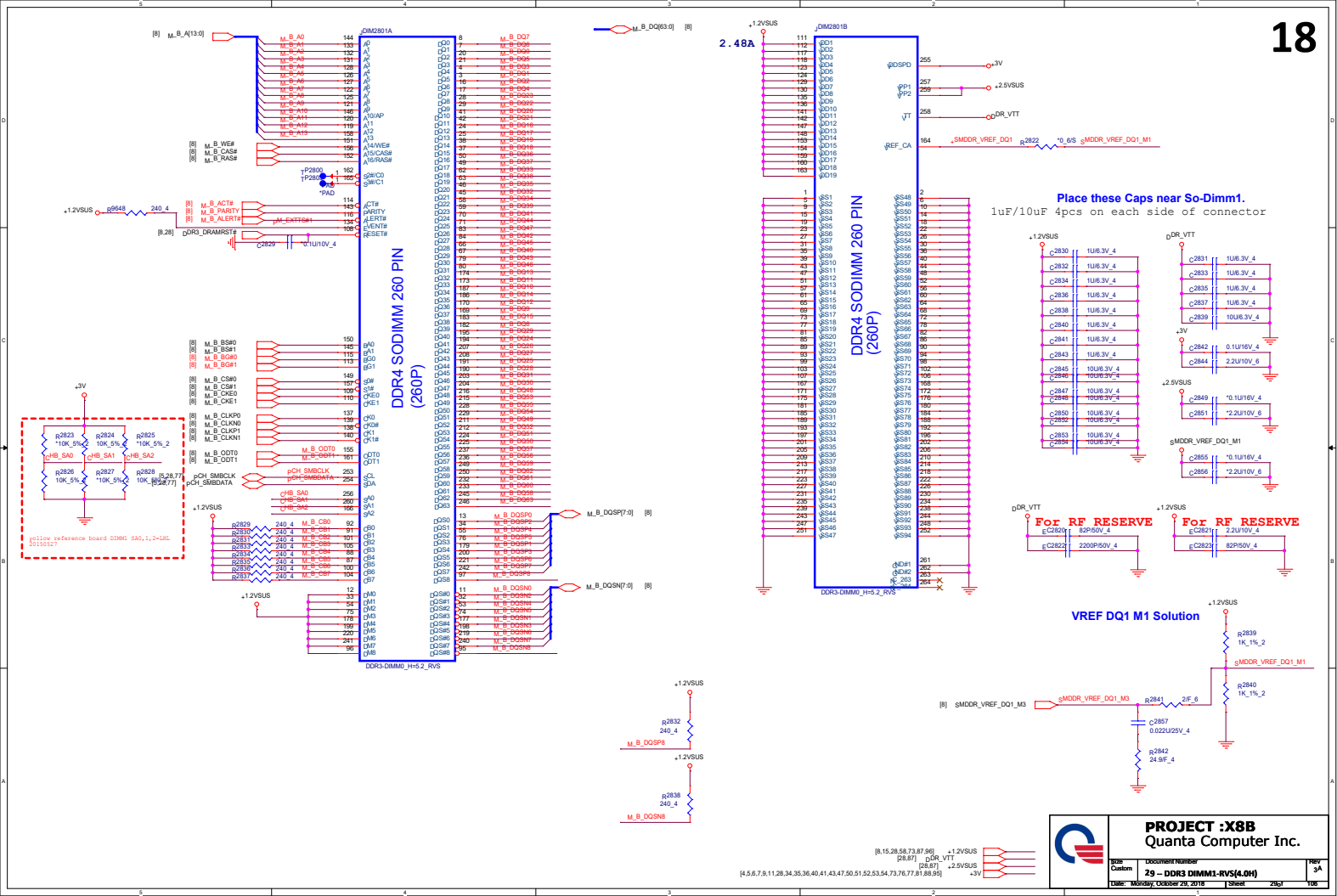
0: PEG WAIT FOR BIOS FOR TRAINING

[11,77]	CFG0	R632	1K_1%_2	
[11,77]	CFG1	R633	1K_1%_2	
[11,77]	CFG2	R634	1K_1%_2	
[11,77]	CFG3	R635	1K_1%_2	
[11,77]	CFG5	R637	1K_1%_2	
[11,77]	CFG6	R638	1K_1%_2	
[11,77]	CFG7	R639	1K_1%_2	
[11,77]	CFG8	R640	1K_1%_2	
[11,77]	CFG9	R641	1K_1%_2	
[11,77]	CFG10	R642	1K_1%_2	
[11,77]	CFG11	R643	1K_1%_2	
[11,77]	CFG12	R644	1K_1%_2	
[11,77]	CFG13	R645	1K_1%_2	
[11,77]	CFG14	R646	1K_1%_2	
[11,77]	CFG15	R647	1K_1%_2	

PROJECT :X8B
Quanta Computer Inc.

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Custom	16 – WHL/CNL (GND)	3A
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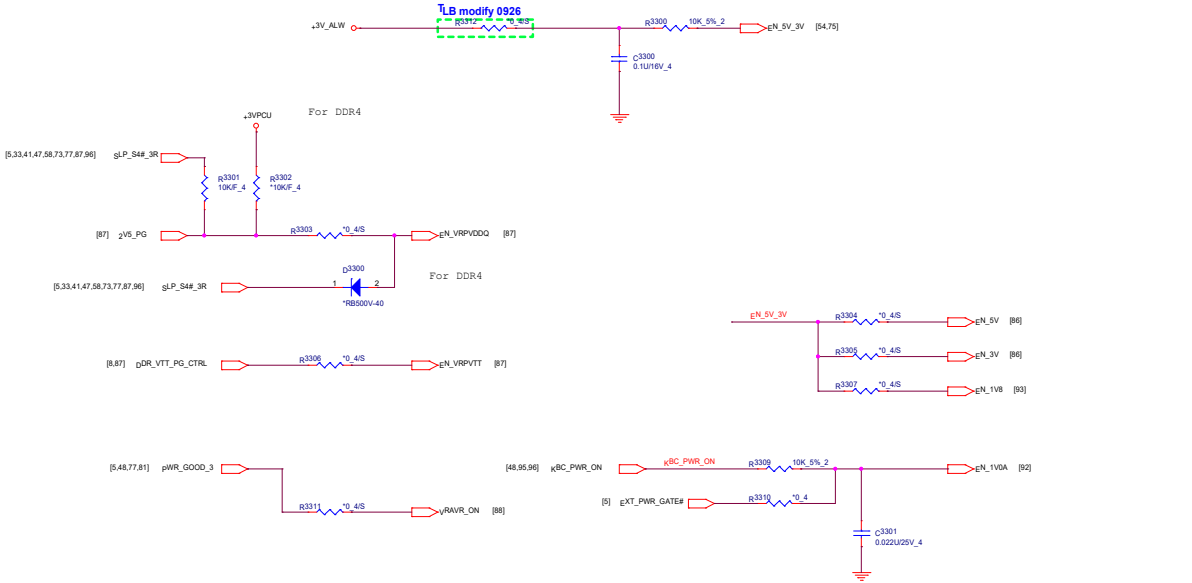

DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=4_RVS
2.48A
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
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PROJECT :X8B
Quanta Computer Inc.
2g – DDR4 DIMM0-STD(4.0H)
Monday, October 29, 2018



PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29 – DDR3 DIMM1-RVS(4.0H)	3A
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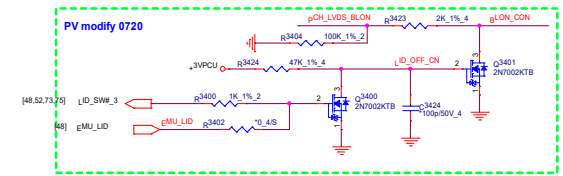
POWER TO EE NET NAME CONNECTION

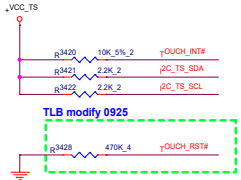


PROJECT :X8B
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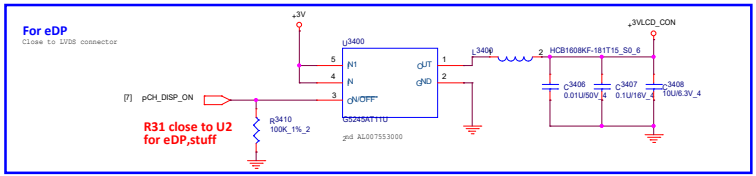
Size	Document Number	Rev
Custom	3 – POWER ENABLE	3A
Date: Monday, October 29, 2018	Sheet 33 of 106	

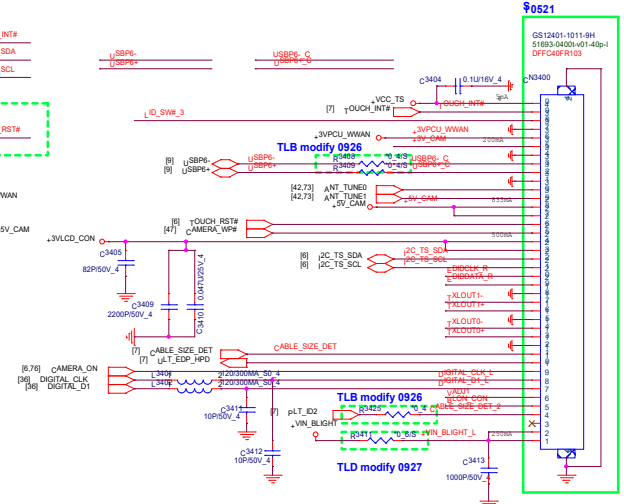
LID Switch

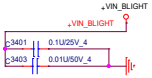




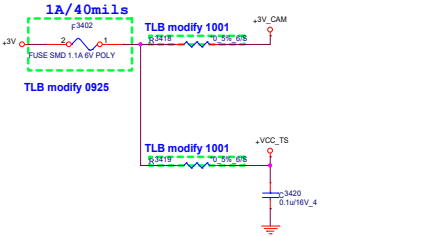


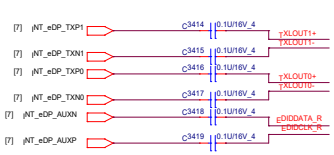


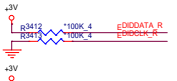




Touch screen







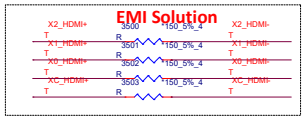


[4,5,6,7,9,11,28,29,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95]
[10,35,36,44,50,54,61,73,81,95]
[73,81,82,86,87,93,97]
+3V
+5V
+VIN

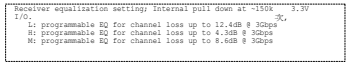
PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3A -- LCD CONN/LID/CAM/D-MIC	3A

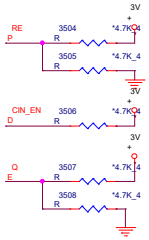
Date: Monday, October 29, 2018 Sheet 34 of 106

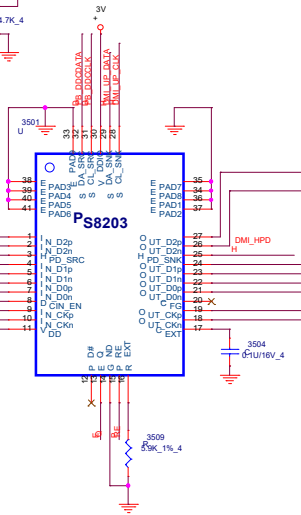


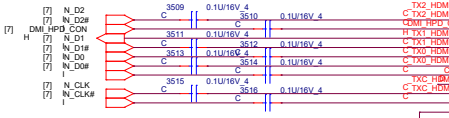


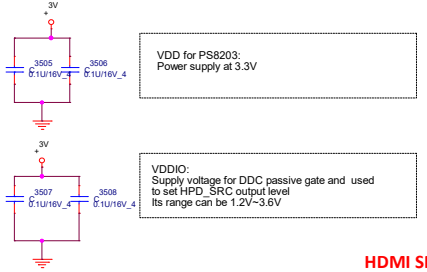


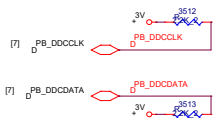


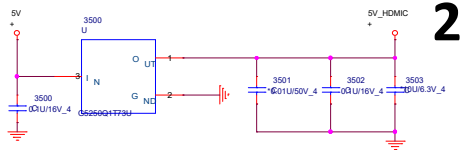


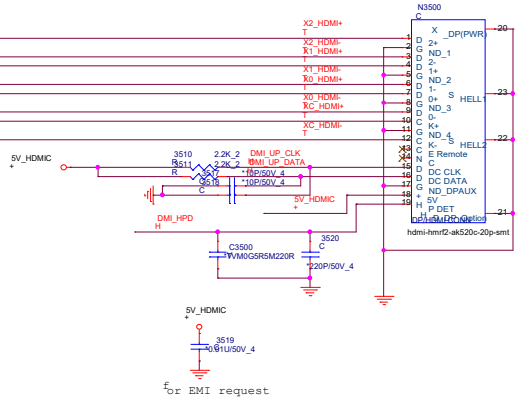






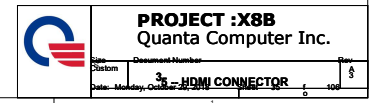


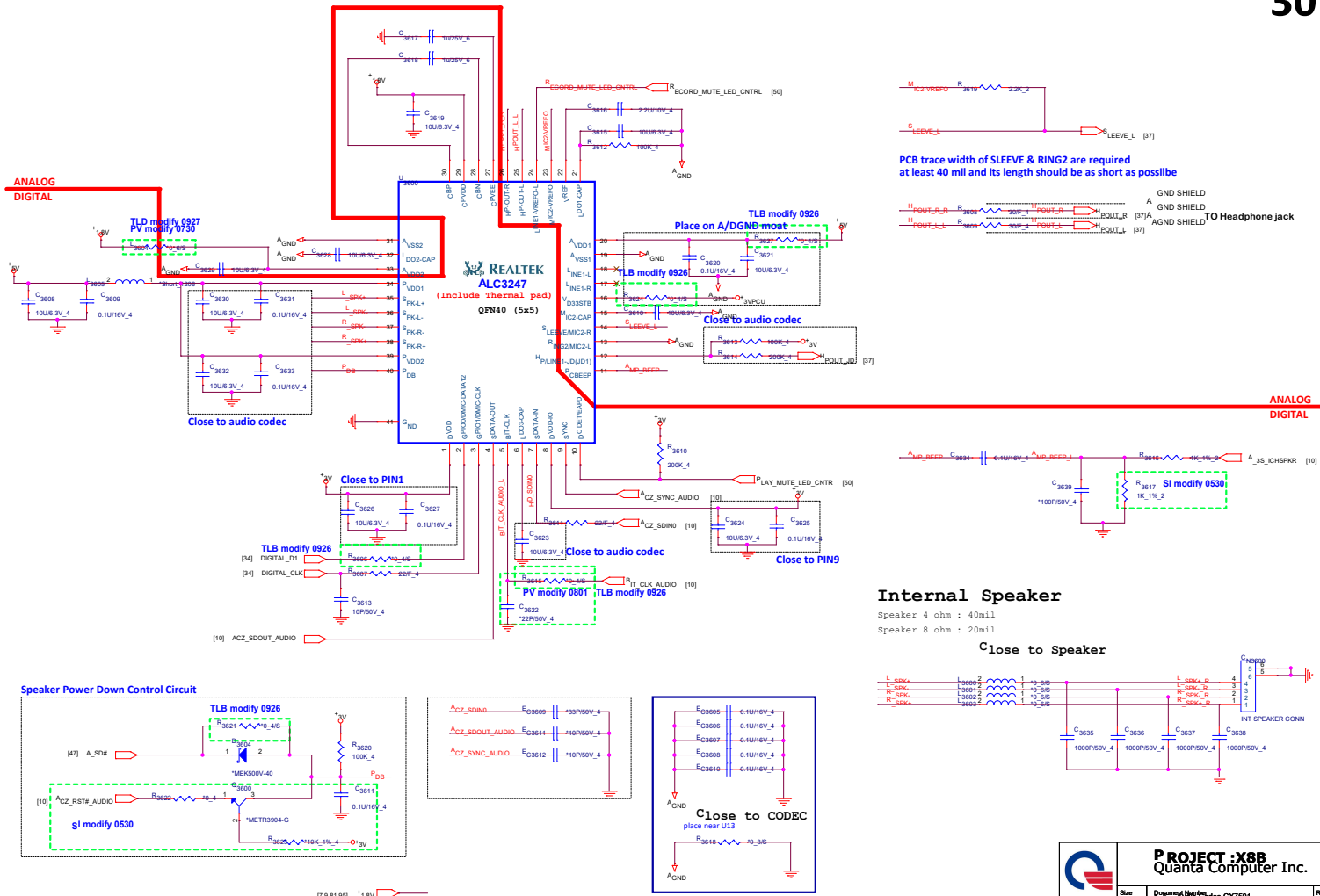




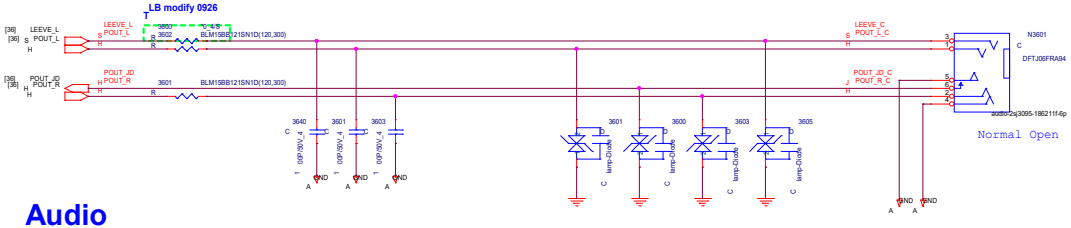
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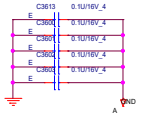


PROJECT : X8B	
Quanta Computer Inc.	
Size: Custom	Document Number: 3_6 — Audio Codec CX7501
Rev: A	
Date: Monday, October 29, 2018	Sheet 36 of 106



Audio

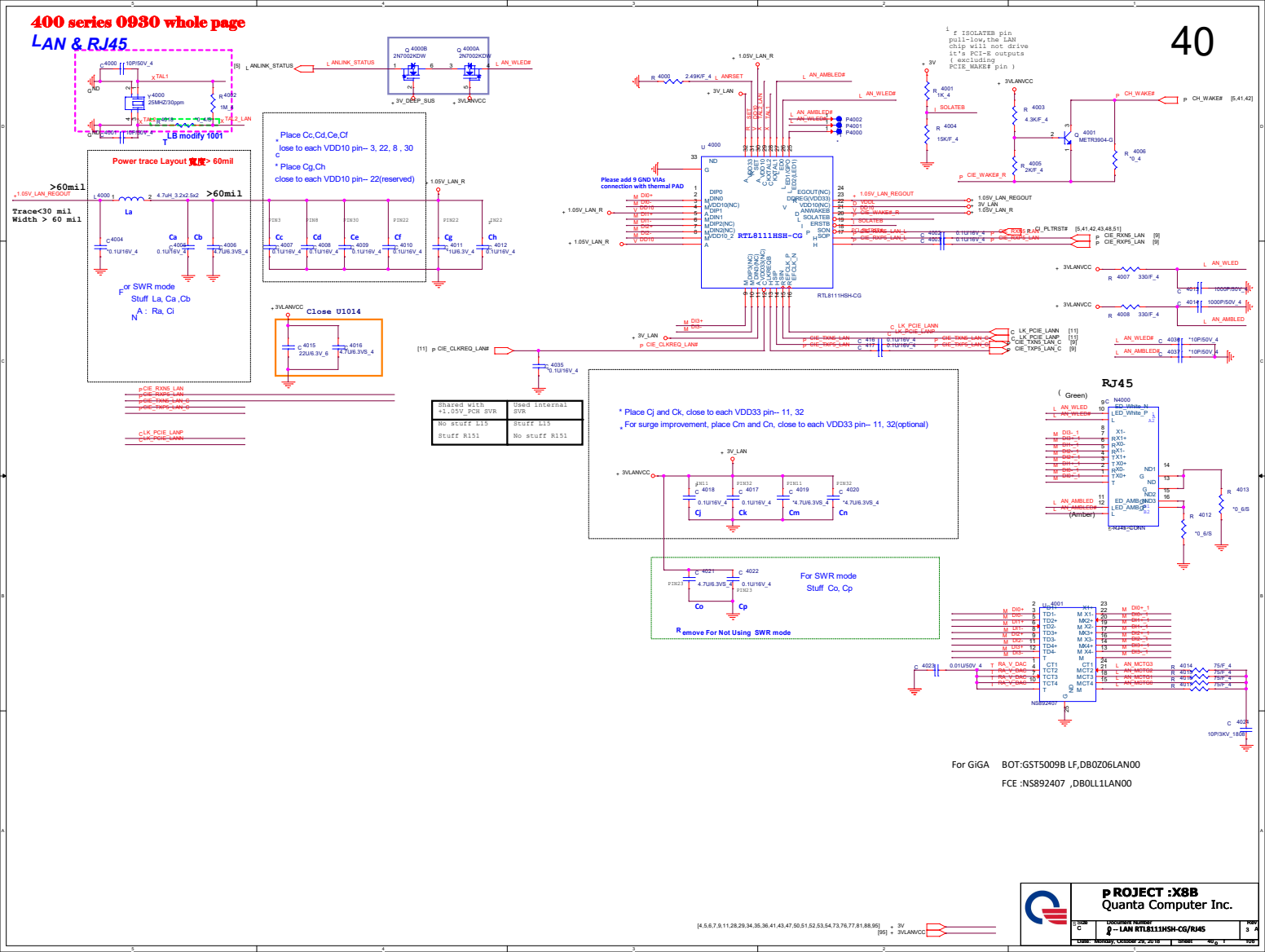
All Clamp-Diode need close to ADO Jack.



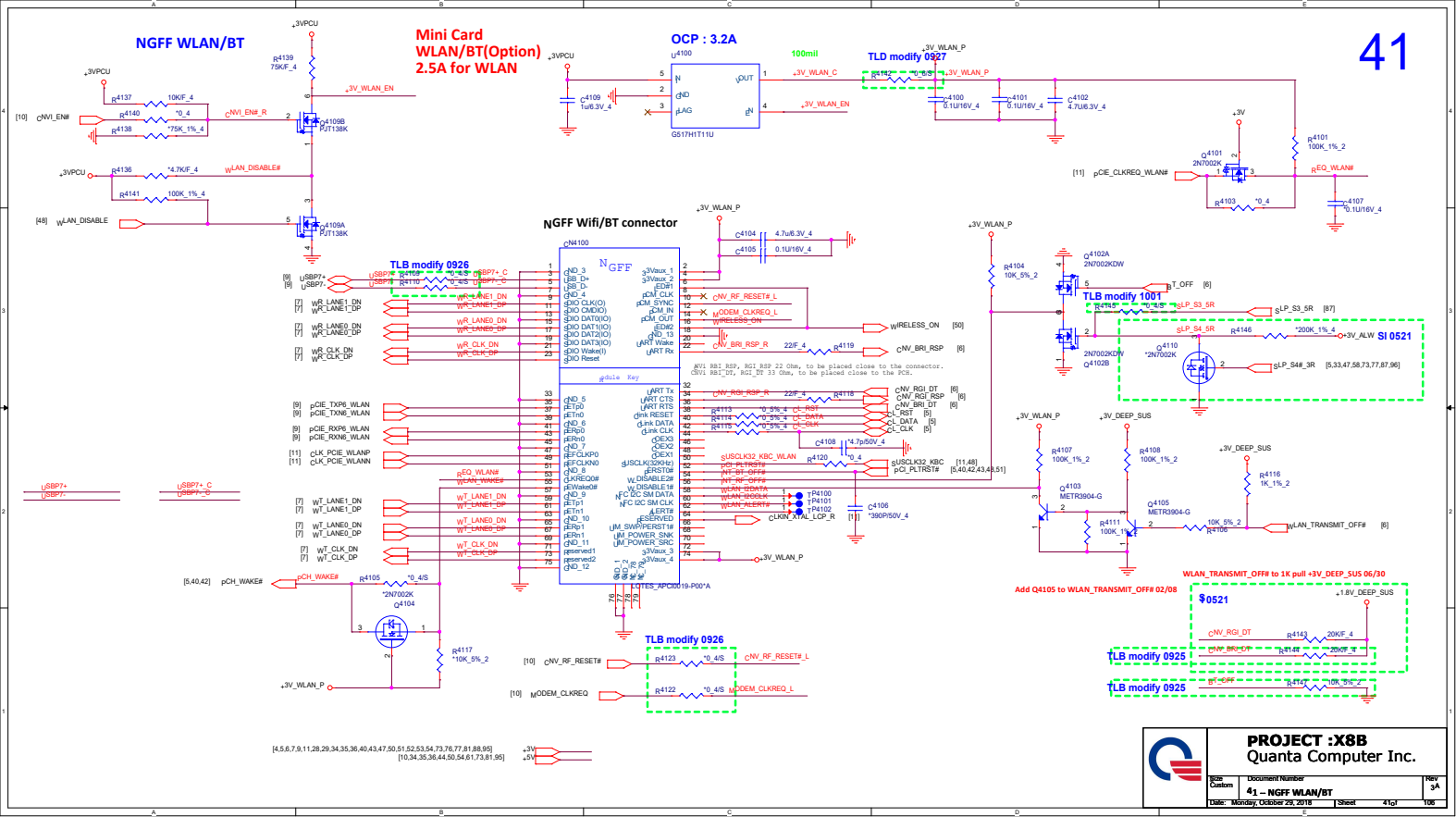
PROJECT :X8B
Quanta Computer Inc.

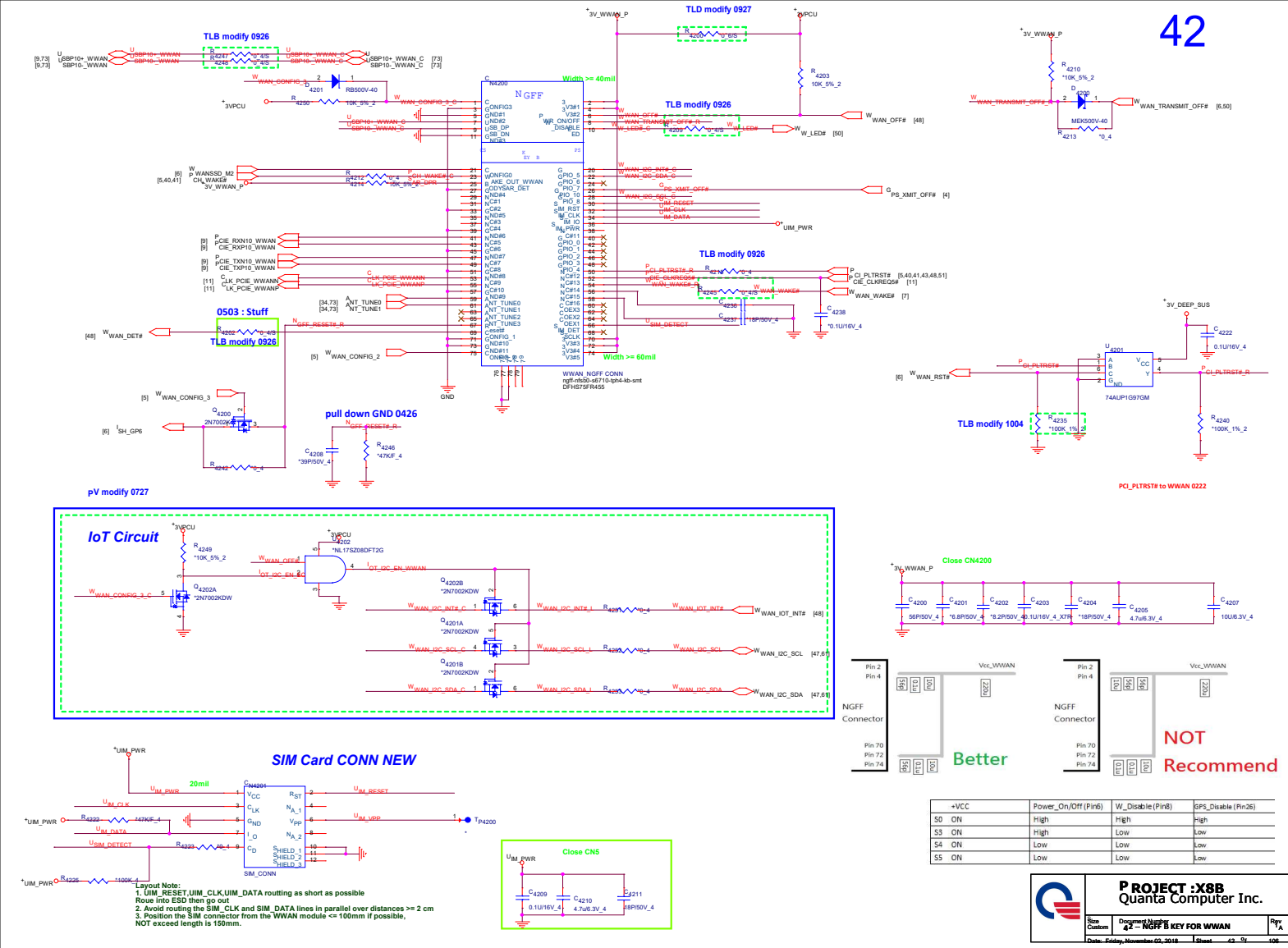
Size	Document Number	Rev
Custom	3	A
Date: Monday, October 29, 2018	Sheet 37 of 38	

Audio JACK



PROJECT :	X8B
Quanta Computer Inc.	
Size: C	Document Number: LAN RTL8111HSH-CG/RJ45
Rev: 3 A	
Date: Monday, October 29, 2018	Sheet 40 of 51


NGFF WLAN/BT
Mini Card
WLAN/BT(Option)
2.5A for WLAN
OCP : 3.2A
100mil
TLD modify 0927
NGFF Wifi/BT connector
TLB modify 0926
TLB modify 1001
TLB modify 0925
Add Q4105 to WLAN_TRANSMIT_OFF# 02/08
WLAN_TRANSMIT_OFF# to 1K pull +3V_DEEP_SUS 06/30
PROJECT :X8B
Quanta Computer Inc.
41 – NGFF WLAN/BT

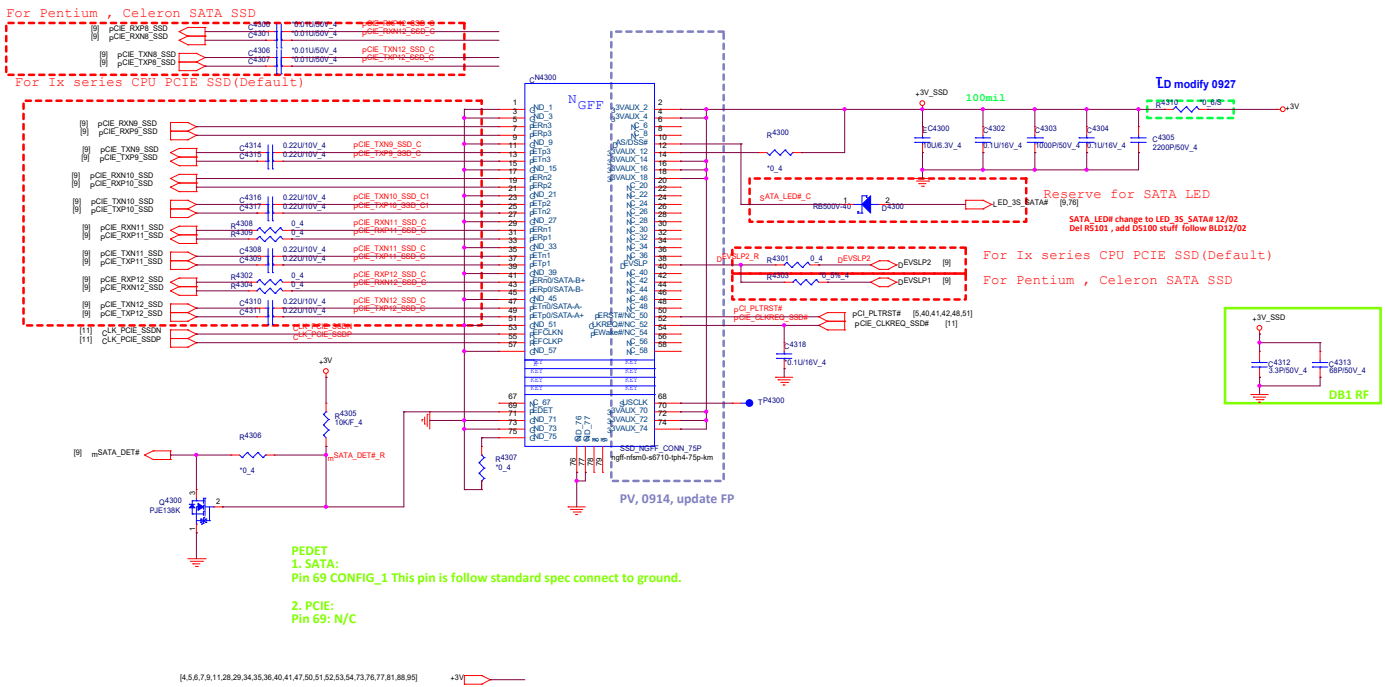


+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0	ON	High	High
S3	ON	High	Low
S4	ON	Low	Low
S5	ON	Low	Low

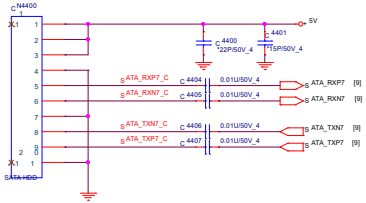
Layout Note:
1. UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible
Roue into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances >= 2 cm
3. Position the SIM connector from the WWAN module <= 100mm if possible,
NOT exceed length is 150mm.

PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	42 – NGFF B KEY FOR WWAN	1A
Date: Friday, November 02, 2018	Sheet 42 of 106	


For Pentium , Celeron SATA SSD
For Ix series CPU PCIE SSD(Default)
N4300
NGFF
ngff-nfsm0-s6710-tph4-75p-km
SSD_NGFF_CONN_75P
+3V_SSD
100mil
LD modify 0927
Reserve for SATA LED
SATA_LED# change to LED_3S_SATA# 12/02
Del R5101 , add DS100 stuff follow BLD12/02
For Ix series CPU PCIE SSD(Default)
For Pentium , Celeron SATA SSD
DB1 RF
PV, 0914, update FP
PEDET
1. SATA:
Pin 69 CONFIG_1 This pin is follow standard spec connect to ground.
2. PCIE:
Pin 69: N/C

SATA-HDD





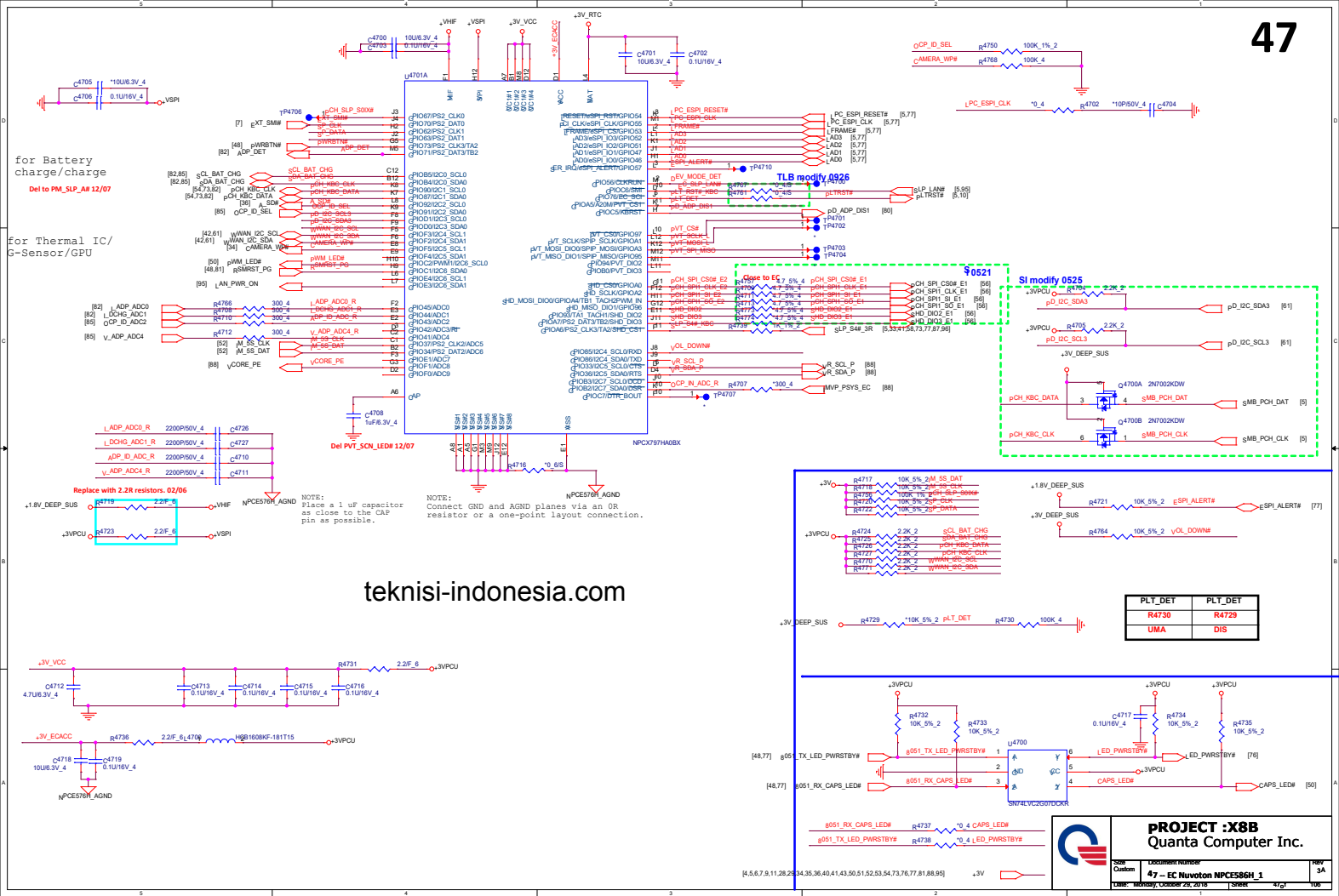
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[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95] +3V
[10,34,35,36,50,54,61,73,81,95] +5V

PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
C	-- HDD/ EMI cap	3 A

Date: Monday, October 29, 2018 Sheet 44 of 47



PROJECT :X8B			
Quanta Computer Inc.			
Size: Custom	Document Number: 47 – EC Nuvoton NPCE586H_1		Rev: 3A
Date: Monday, October 29, 2018	Sheet: 47 of 106		

All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power

EC

TLB modify 0926
SI 0521

change to EC Table 12/07

TLB modify 0926
SI 0521

TLB modify 0926
SI 0521

U4701B
NPCX797HA0BX

CPU I/O Rail Power Supply

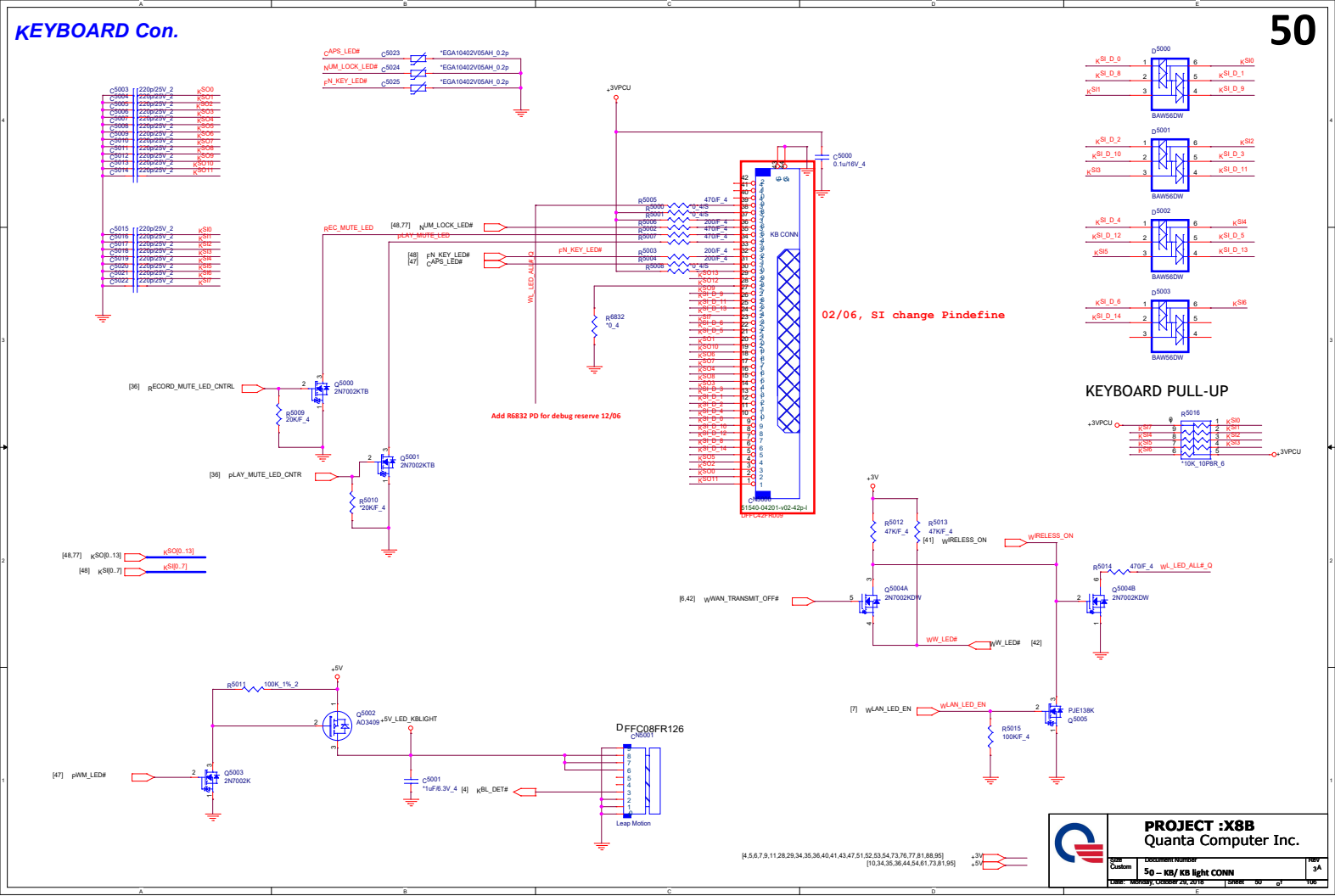
ESD SOLUTION

TLB modify 1004

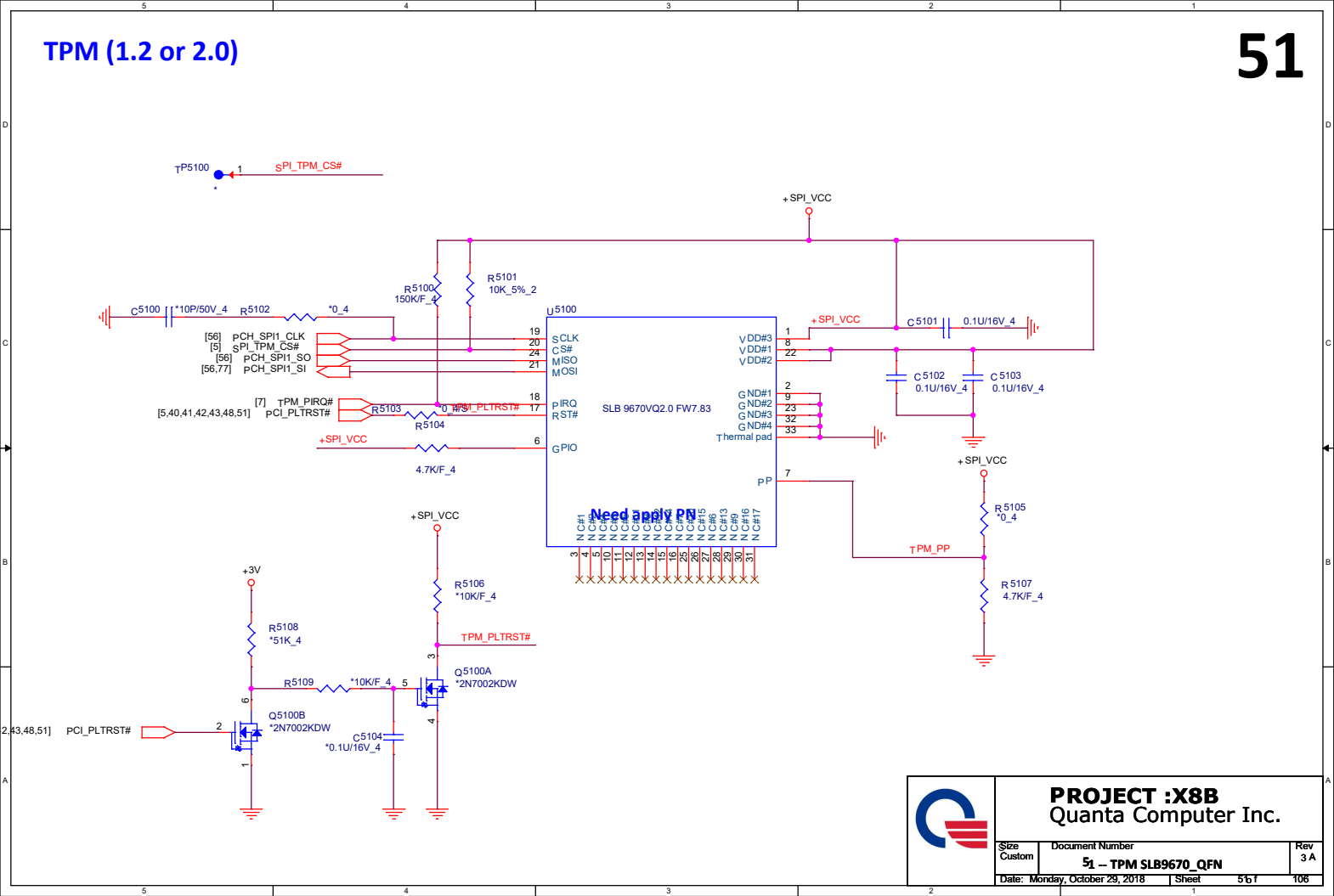
SI modify 0604

Q4701
2N7002K

NOTE : IF INSTALL R10603, PLEASE UNINSTALL R224

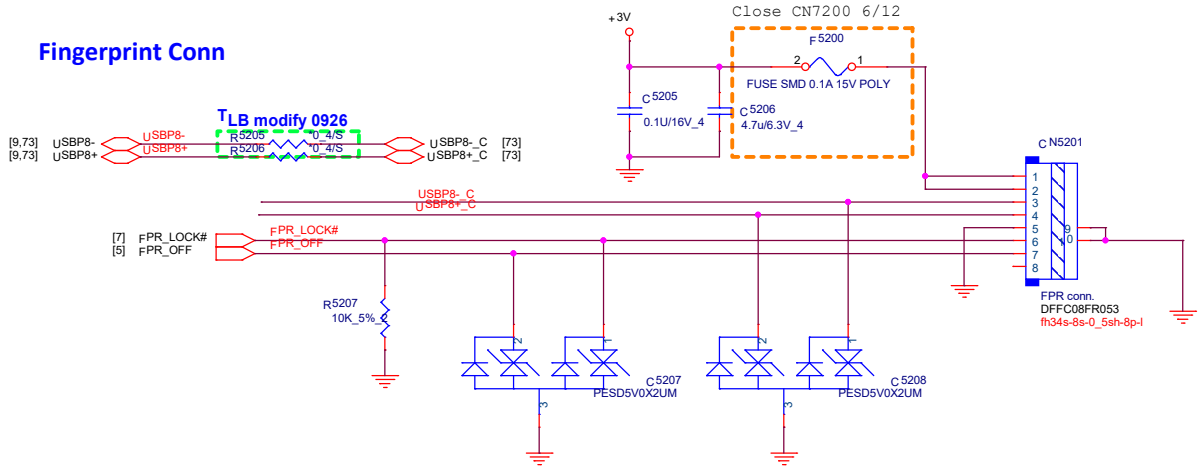

02/06, SI change Pindefine
Add R6832 PD for debug reserve 12/06
KEYBOARD PULL-UP
KB CONN
Leap Motion
BAW56DW
*10K_10P8R_6
PROJECT :X8B
Quanta Computer Inc.
5σ – KB/ KB light CONN
Monday, October 29, 2018

TPM (1.2 or 2.0)

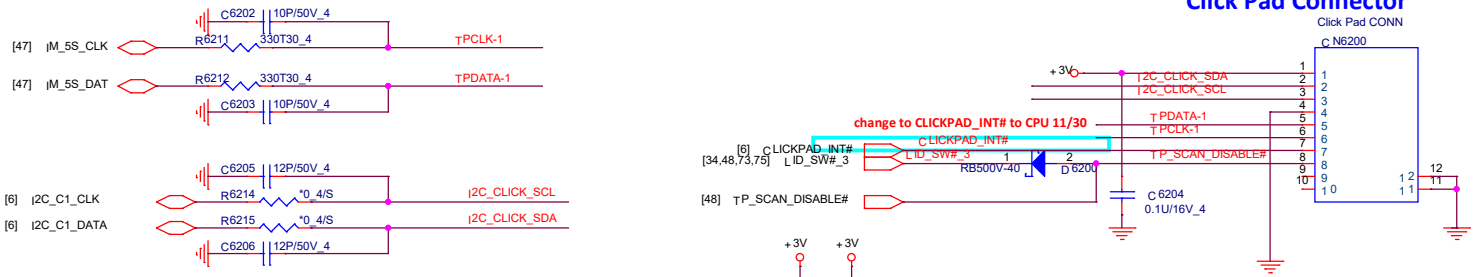


PROJECT :X8B Quanta Computer Inc.			
Size: Custom	Document Number: 51 – TPM SLB9670_QFN		Rev: 3 A
Date: Monday, October 29, 2018	Sheet: 51 of 106		

Fingerprint Conn



Click Pad Connector

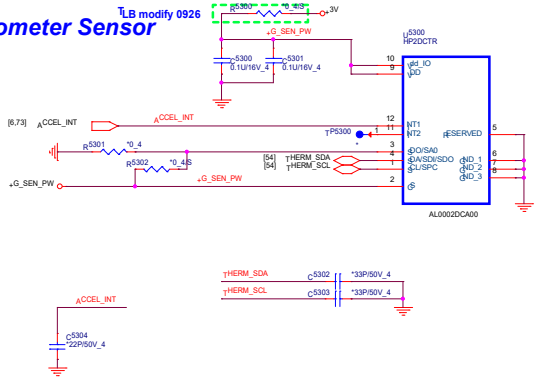


CLICK PAD
Address: 0x20(7 bit)

PROJECT :X8B Quanta Computer Inc.		
Size: Custom	Document Number: 52 – FPR / Click PAD	Rev: 3 A
Date: Monday, October 29, 2018	Sheet 52 of 106	

Accelerometer Sensor

TLB modify 0926



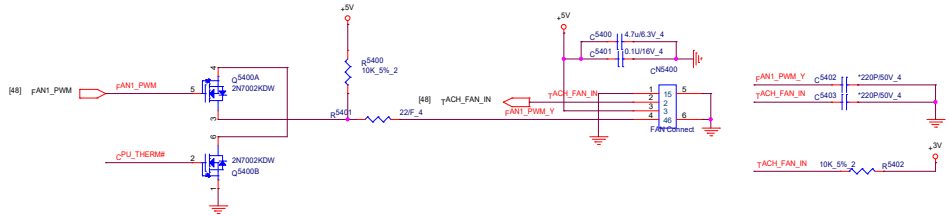
[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,54,73,76,77,81,88,95] +3V

[5,7,12,33,34,36,41,42,47,48,50,54,58,61,73,75,77,80,81,82,85,86,87,88,92,93,95] +3VPCU

PROJECT :X8B
Quanta Computer Inc.

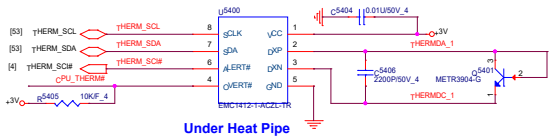
Size	Document Number	Rev
Custom	53 -- TS and Accelerometer	3A
Date: Monday, October 29, 2018	Sheet 53 of 108	

FAN



Thermal sensor

CPU Thermal Sensor

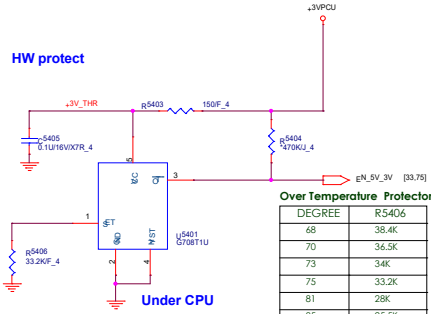


Under Heat Pipe

2nd:AL000431014 TMP431ADGKR

Main: AL000781012 G781P8(98h)

HW protect

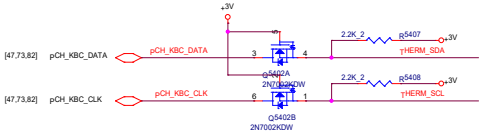


Under CPU

Over Temperature Protecton

DEGREE	R5406	
68	38.4K	CS33832FB08
70	36.5K	
73	34K	CS33402FB18
75	33.2K	CS33322FB13
81	28K	
85	25.5K	CS32552FB11

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147



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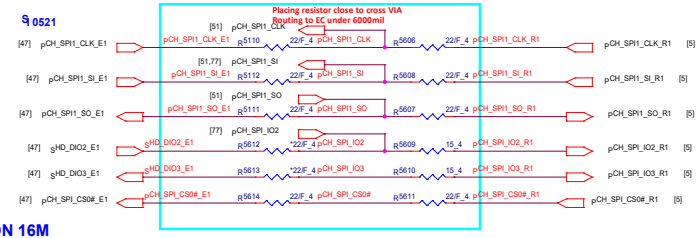
[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,73,76,77,81,88,95]
[11,33,41,73,75,81,85,86,87,93]
+3V
+3V_ALW

PROJECT :X8B
Quanta Computer Inc.

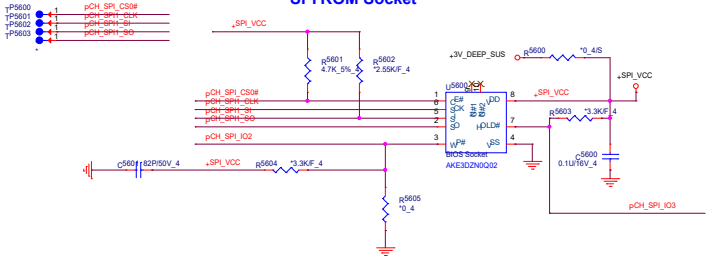
Size	Document Number	Rev
Custom	54– FAN and Thermal IC	3A
Date: Monday, October 29, 2018	Sheet 54 of 106	

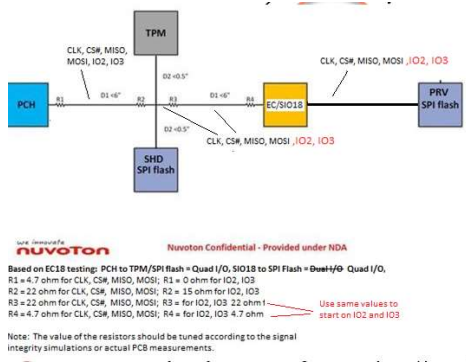
SPI ROM

Vender	Size	P/N	
GD	128MB	AKE2DF00Q00	Pilot run stage
Winbond	128MB	AKE3DF-KN00	
Socket		DFHS08FS046	
GD	128MB	AKE3DZN0Q02	MV stage
Winbond	128MB	AKE3DF-KN01	



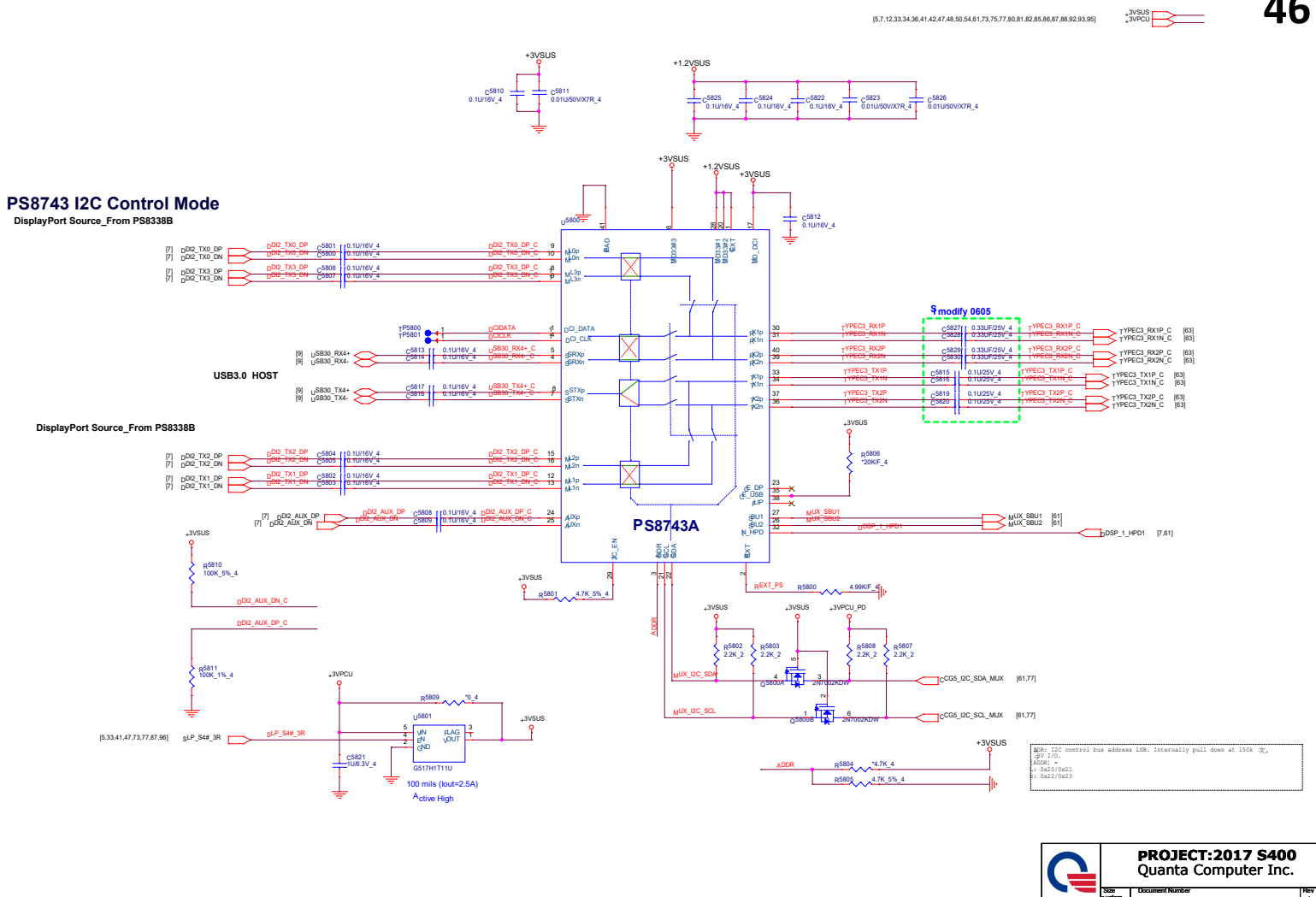
PCH SPI ROM(CLG)
Place TP at TOP side

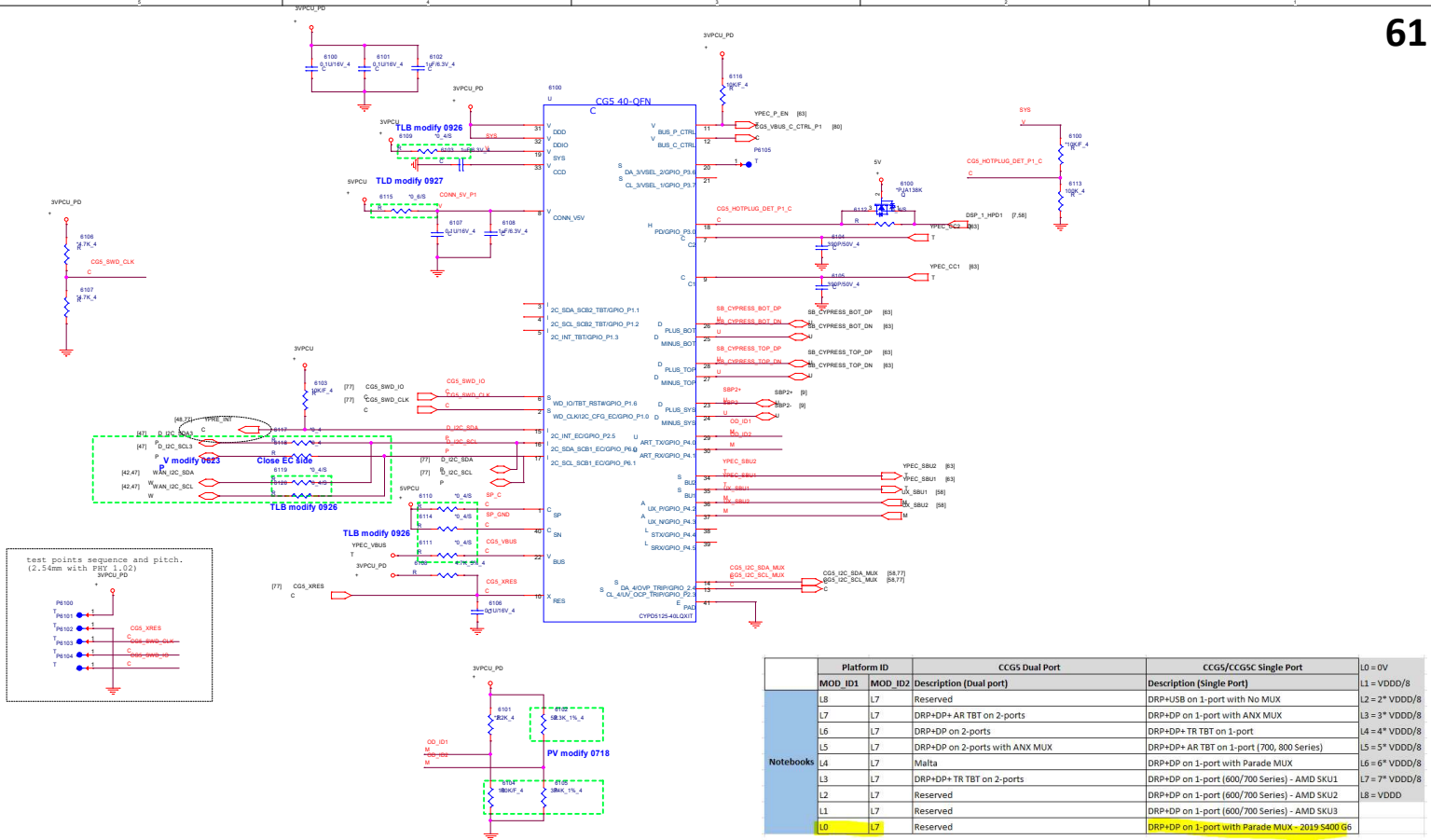




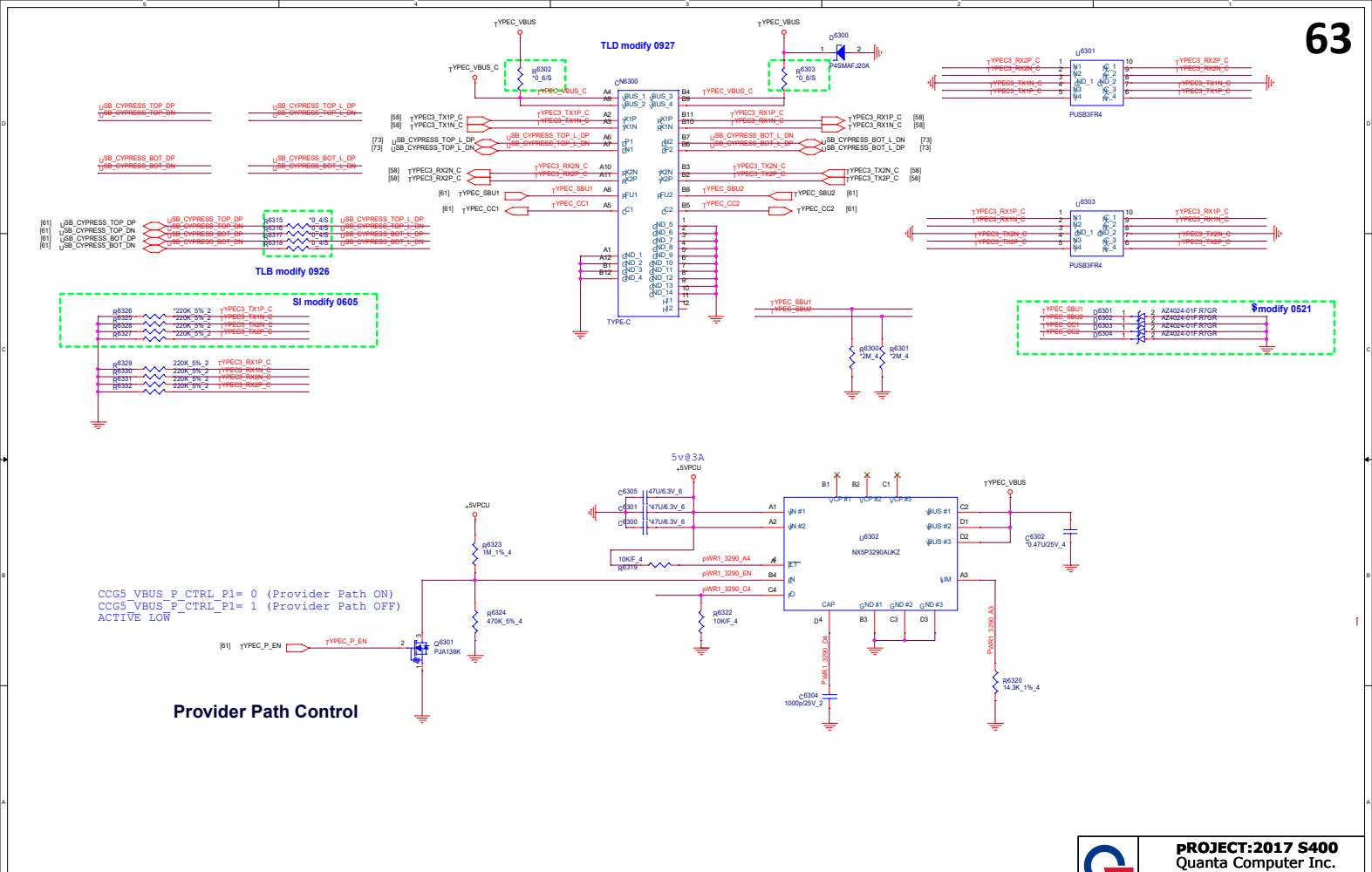
PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	56 – Flash(KBC+PCH)	3A
Date: Monday, October 29, 2018	Sheet 56 of 106	


PS8743 I2C Control Mode
DisplayPort Source_From PS8338B
USB3.0 HOST
DisplayPort Source_From PS8338B
PS8743A
+3VSUS
+1.2VSUS
+3VPCU
modify 0605
100 mils (Iout=2.5A)
Active High
ADDR: I2C control bus address LSB. Internally pull down at 150k 欧, 3V I/O.
[ADDR] =
L: 0x20/0x21
H: 0x22/0x23

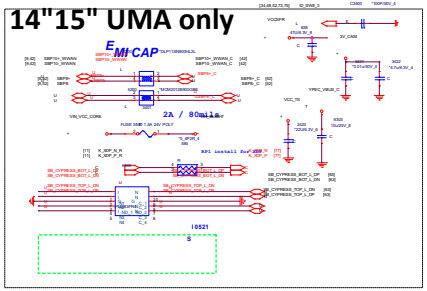


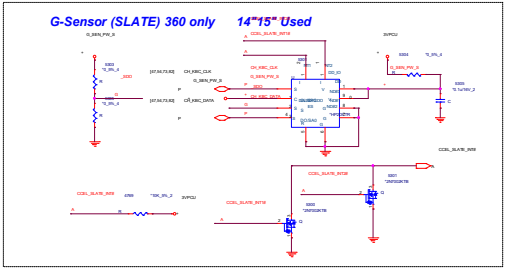
	Platform ID		CCG5 Dual Port	CCG5/CCG5C Single Port	L0 = 0V
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (Single Port)	L1 = VDDD/8
Notebooks	L8	L7	Reserved	DRP+USB on 1-port with No MUX	L2 = 2* VDDD/8
	L7	L7	DRP+DP+ AR TBT on 2-ports	DRP+DP on 1-port with ANX MUX	L3 = 3* VDDD/8
	L6	L7	DRP+DP on 2-ports	DRP+DP+ TR TBT on 1-port	L4 = 4* VDDD/8
	L5	L7	DRP+DP on 2-ports with ANX MUX	DRP+DP+ AR TBT on 1-port (700, 800 Series)	L5 = 5* VDDD/8
	L4	L7	Malta	DRP+DP on 1-port with Parade MUX	L6 = 6* VDDD/8
	L3	L7	DRP+DP+ TR TBT on 2-ports	DRP+DP on 1-port (600/700 Series) - AMD SKU1	L7 = 7* VDDD/8
	L2	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU2	L8 = VDDD
	L1	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU3	
	L0	L7	Reserved	DRP+DP on 1-port with Parade MUX - 2019 S400 G6	

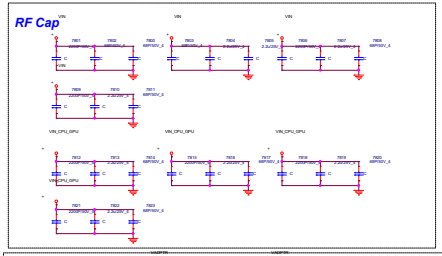


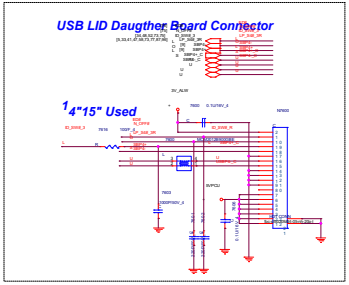
NB5	PROJECT:2017 S400 Quanta Computer Inc.		
Size	Document Number 63 – TYPE-C		Rev 3A
Date:	Monday, October 29, 2018	Sheet	63 of 106

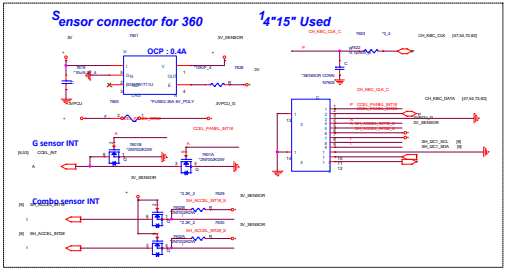
14"15" UMA only

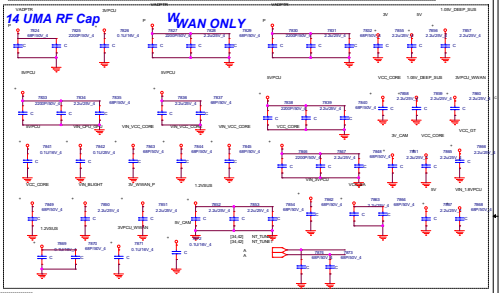


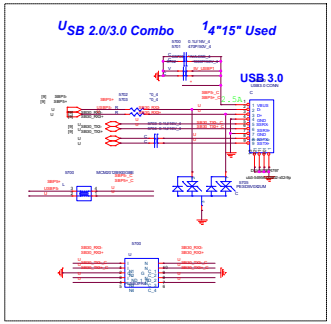


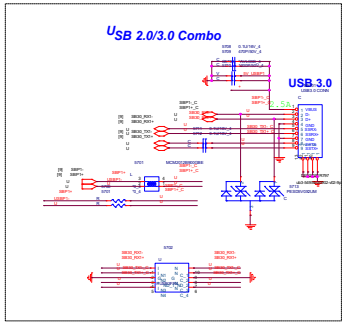


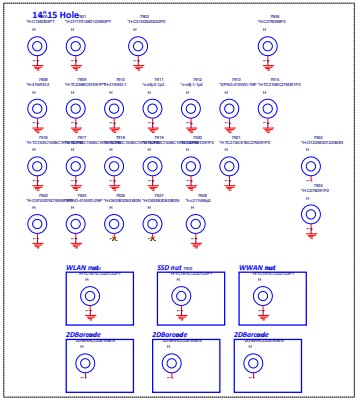




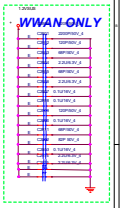


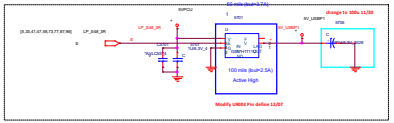






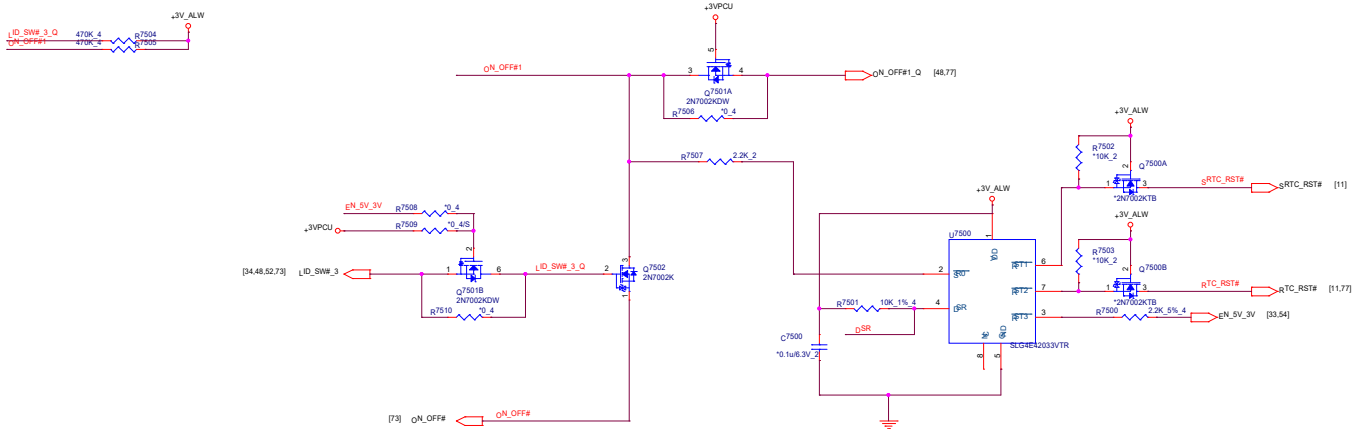
teknisi-indonesia.com





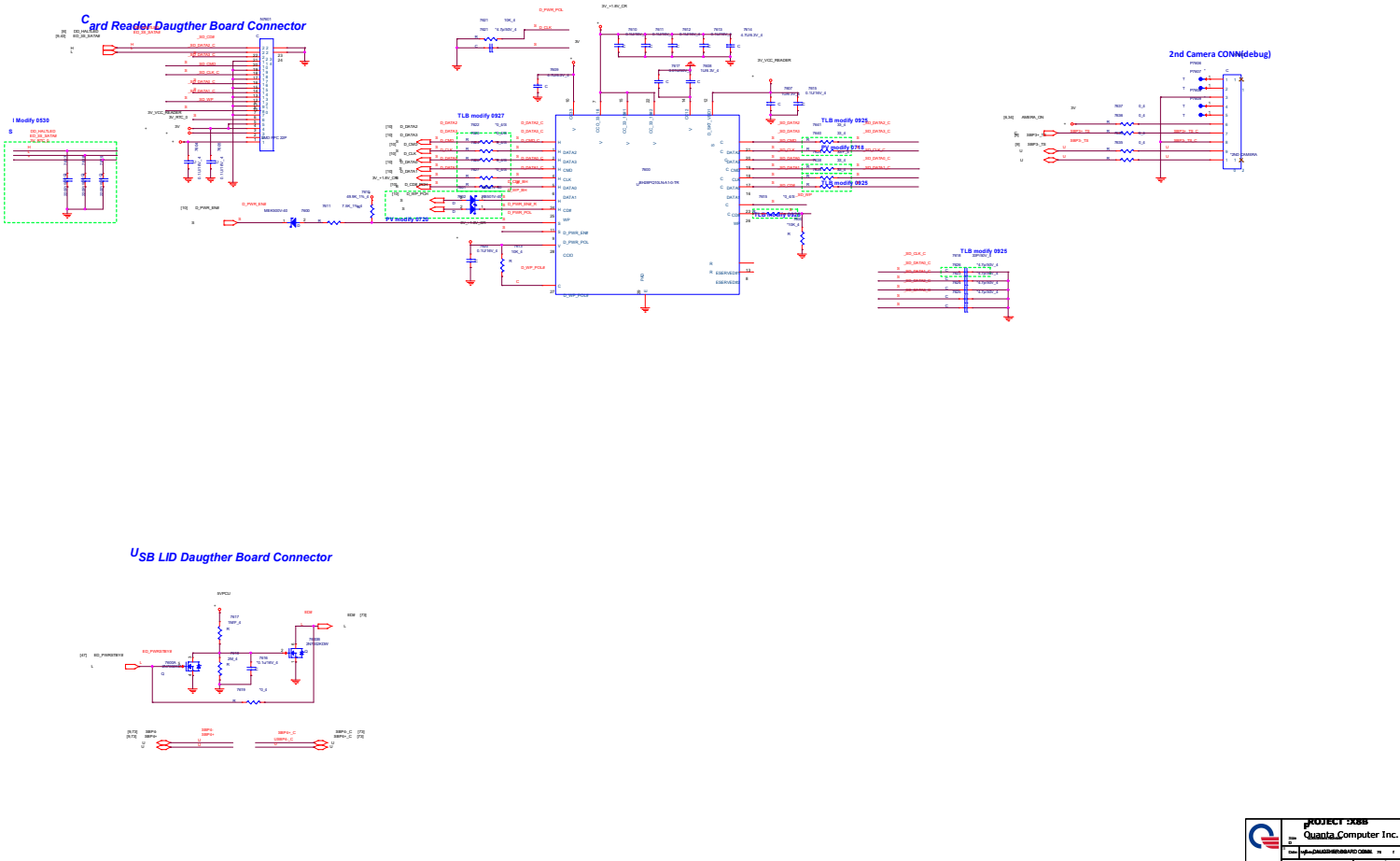
Quanta Computer Inc.	PROJECT : 1XBB		
	D - REPEATER P0040FA		
Date: Friday, December 02, 2016	Sheet 72		

Power Botton Connector

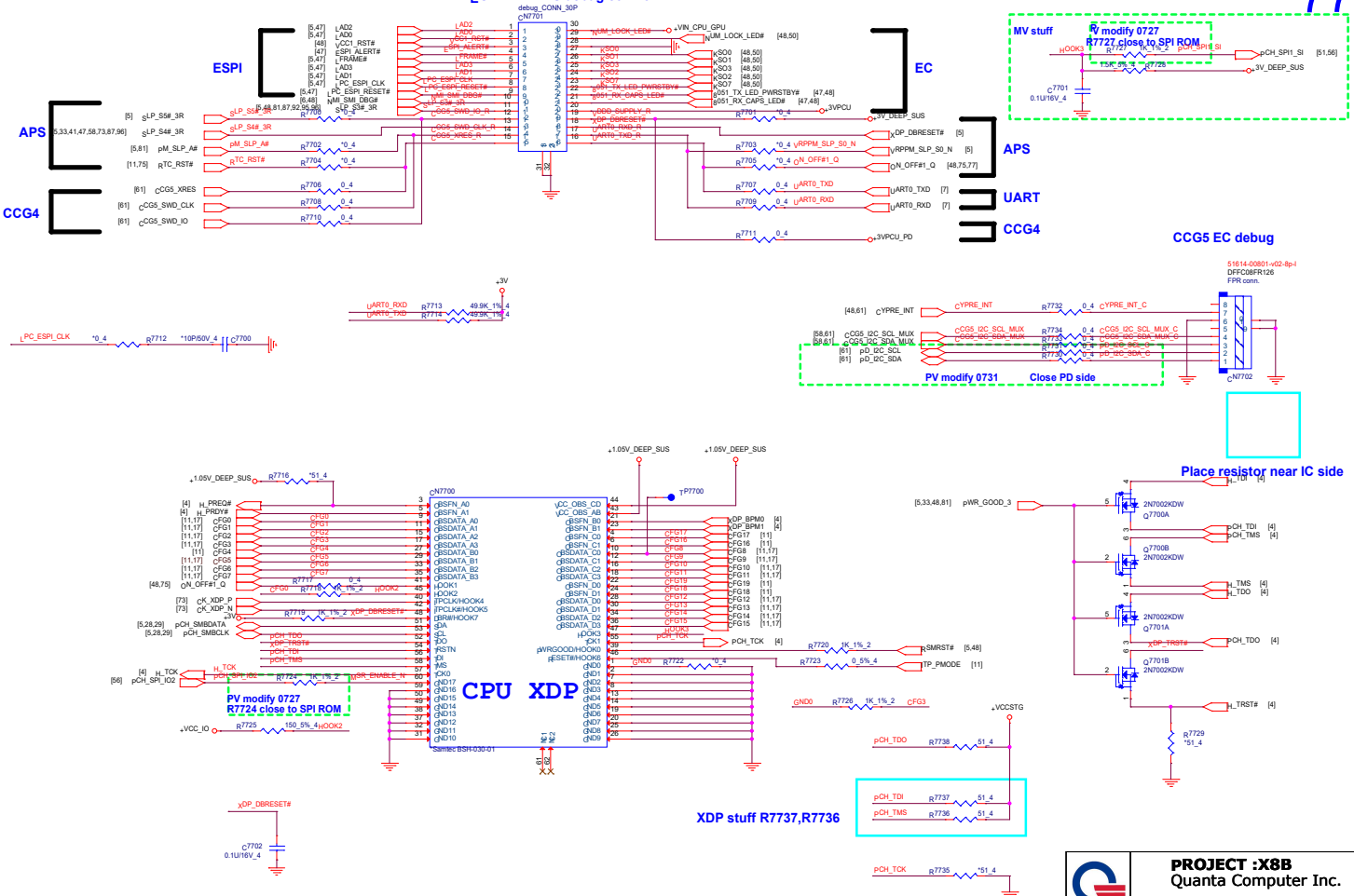


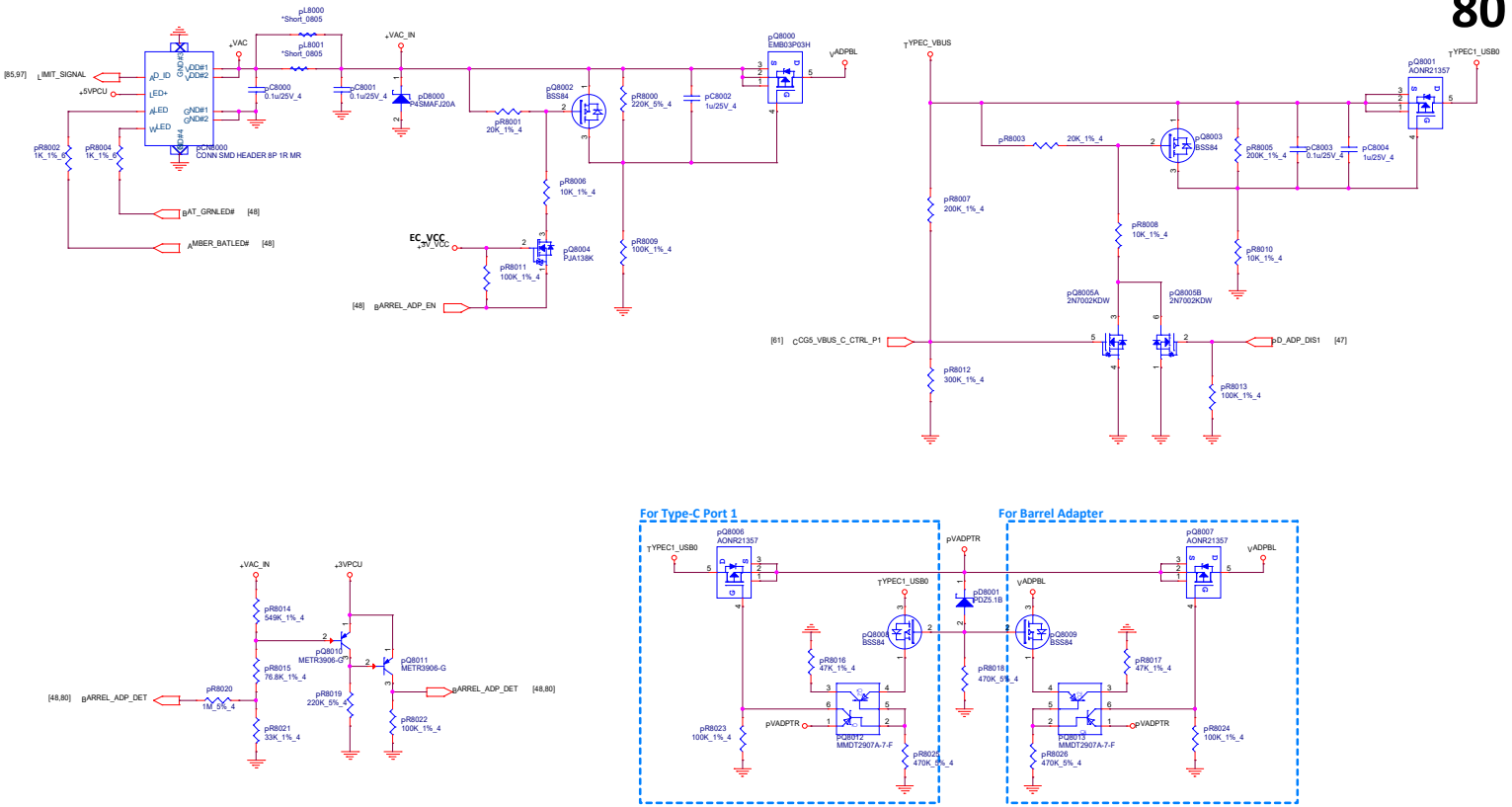
[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95] +3V
[10,34,35,36,44,50,54,61,73,81,95] +5V
[11,33,41,73,81,85,86,87,93] +3V_ALW

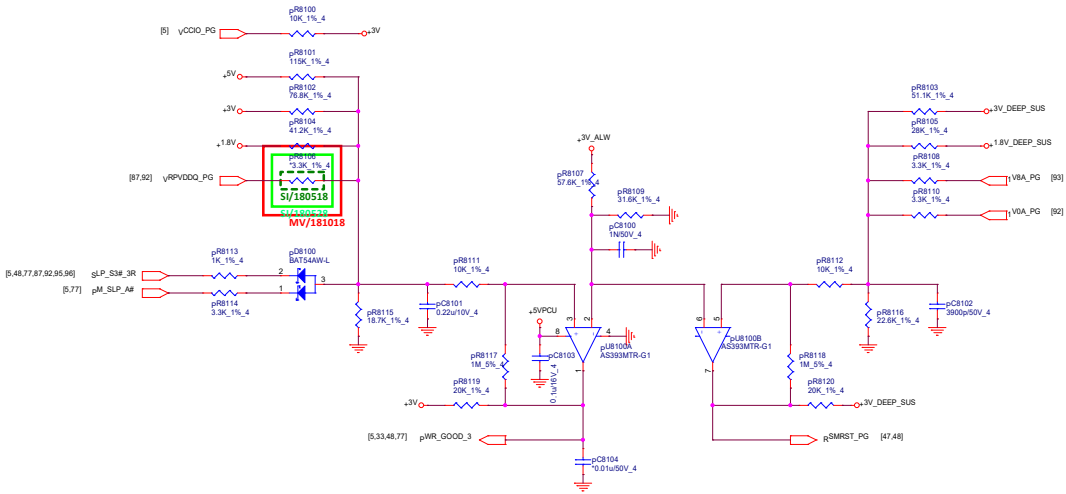
PROJECT :X8B Quanta Computer Inc.		
Size: Custom	Document Number: 75 – Power Button/ HW Reset	Rev: 3A
Date: Monday, October 29, 2018	Sheet: 75 of 106	


Card Reader Daugther Board Connector
2nd Camera CONN(debug)
USB LID Daugther Board Connector
TLB modify 0927
PV modify 0720
TLB modify 0925
PV modify 0716
PV modify 0926
TLB modify 0925
i Modify 0530
PROJECT : X88
Quanta Computer Inc.

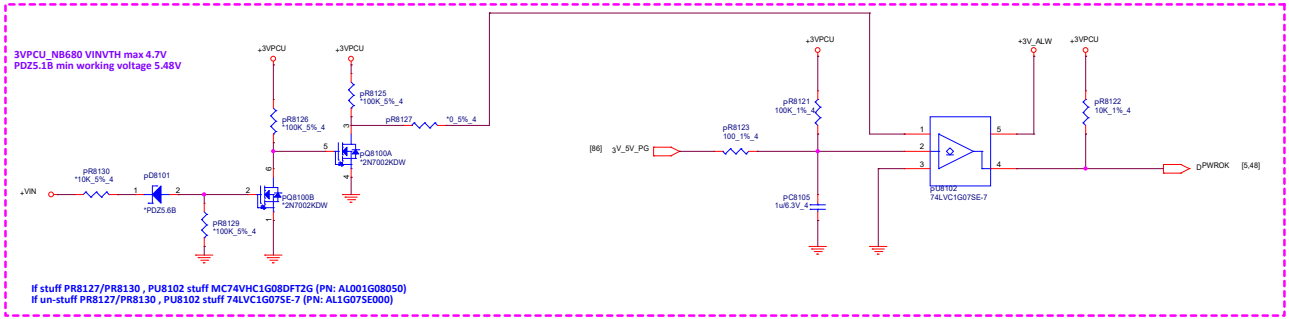
eSPI+EC+APS debug conn on MB




For Type-C Port 1
For Barrel Adapter
PROJECT :X8B
Quanta Computer Inc.
80 – TYPE-C/Barrel switch
Monday, October 29, 2018



PV/180801

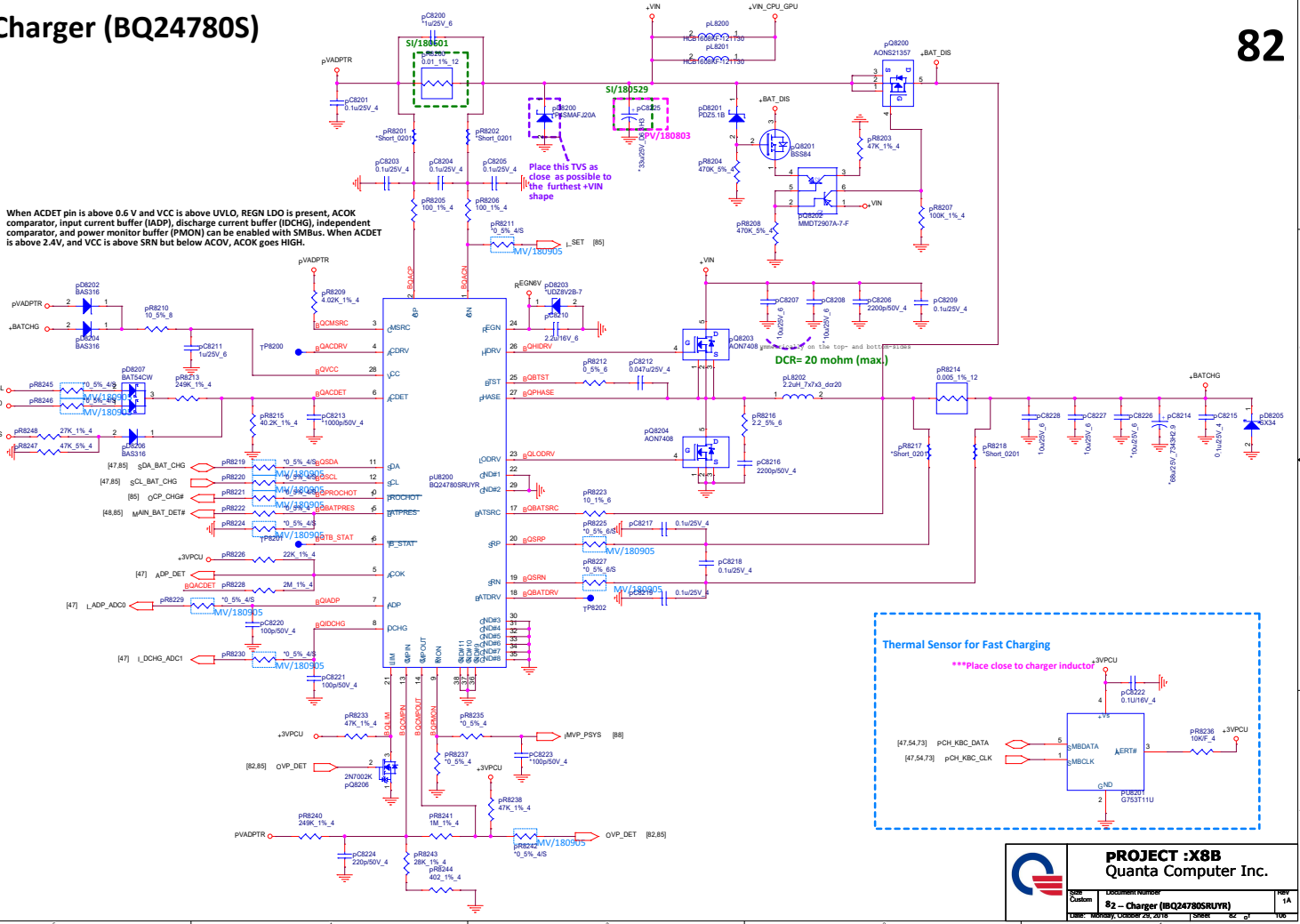


[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,88,95] +3V
[10,34,35,36,44,50,54,61,73,95] +5V
[11,33,41,73,75,85,86,87,93] +3V_ALW

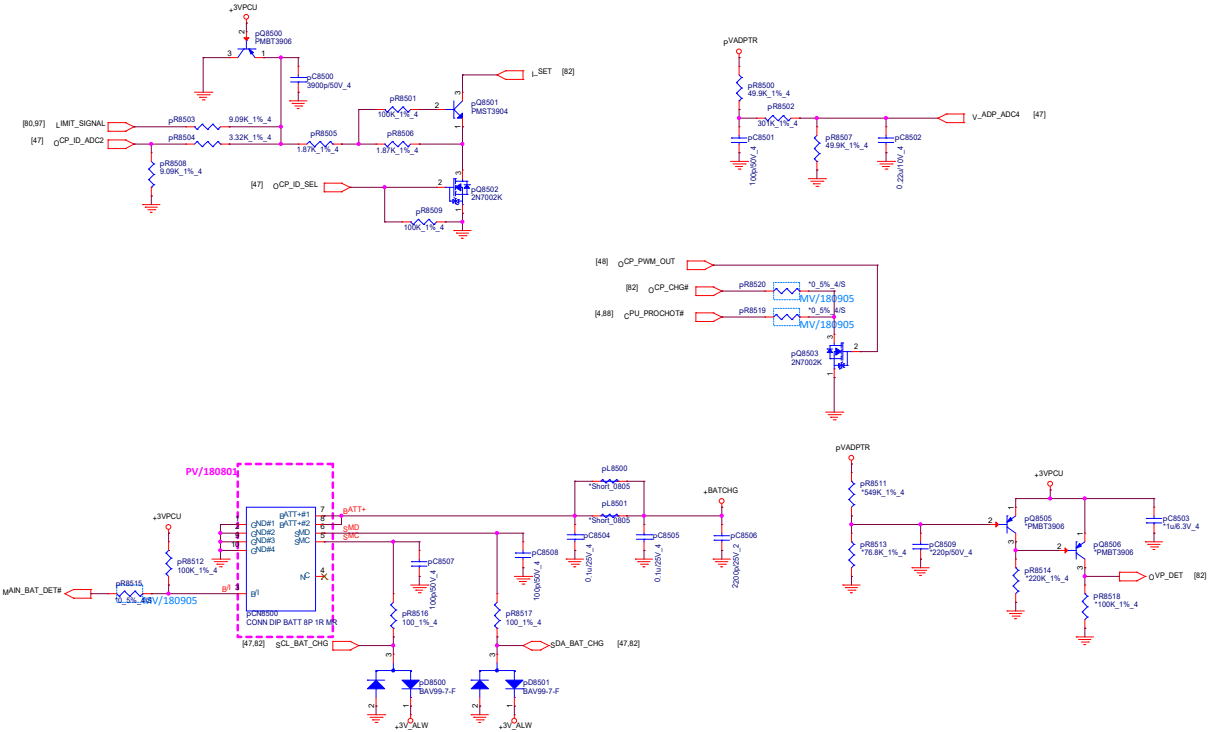
PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	81 – PWROK	1A
Date: Monday, October 29, 2018	Sheet 81 of 105	

Charger (BQ24780S)

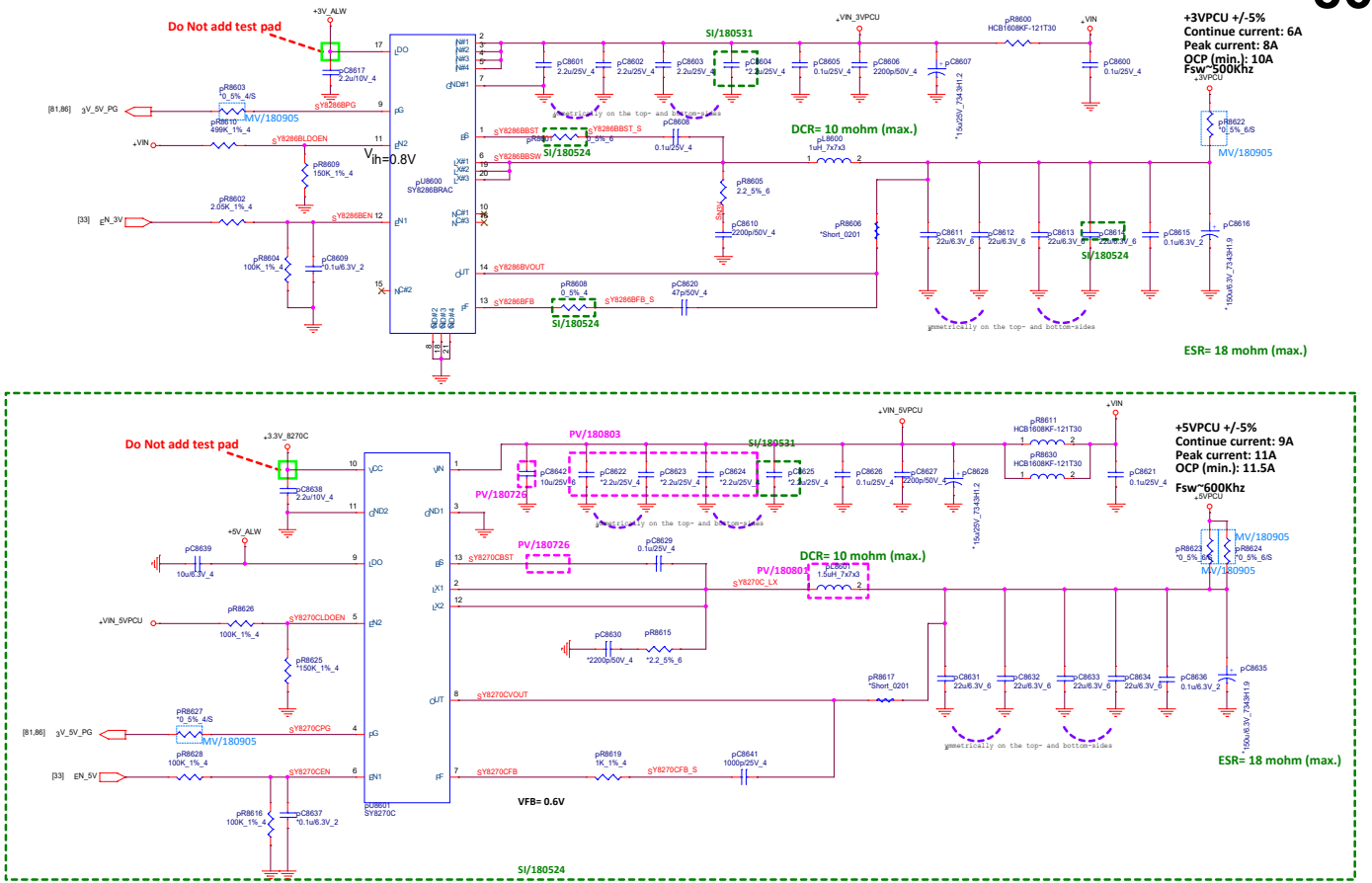


Barrel Adapter OCP



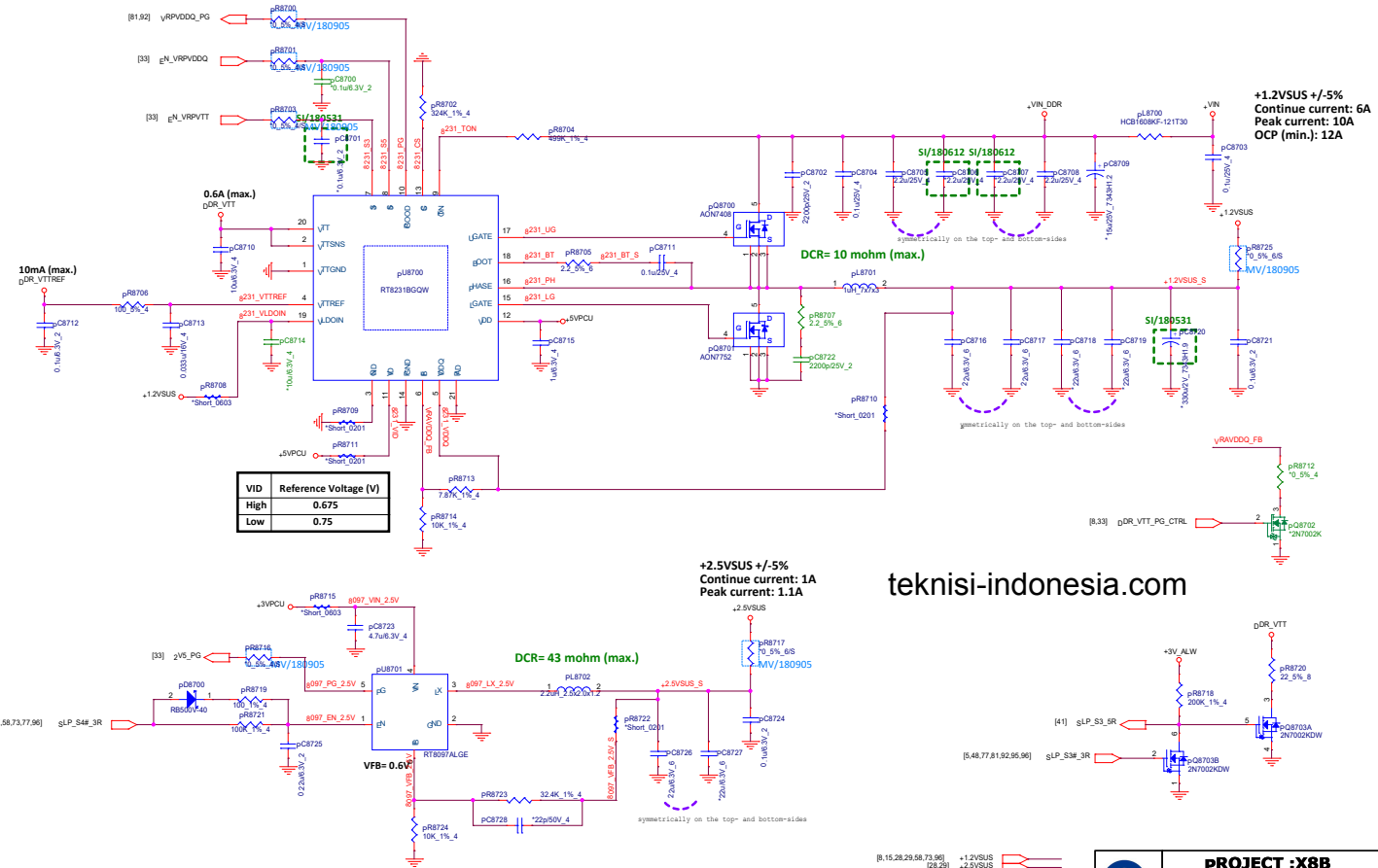
PROJECT :X8B
Quanta Computer Inc.

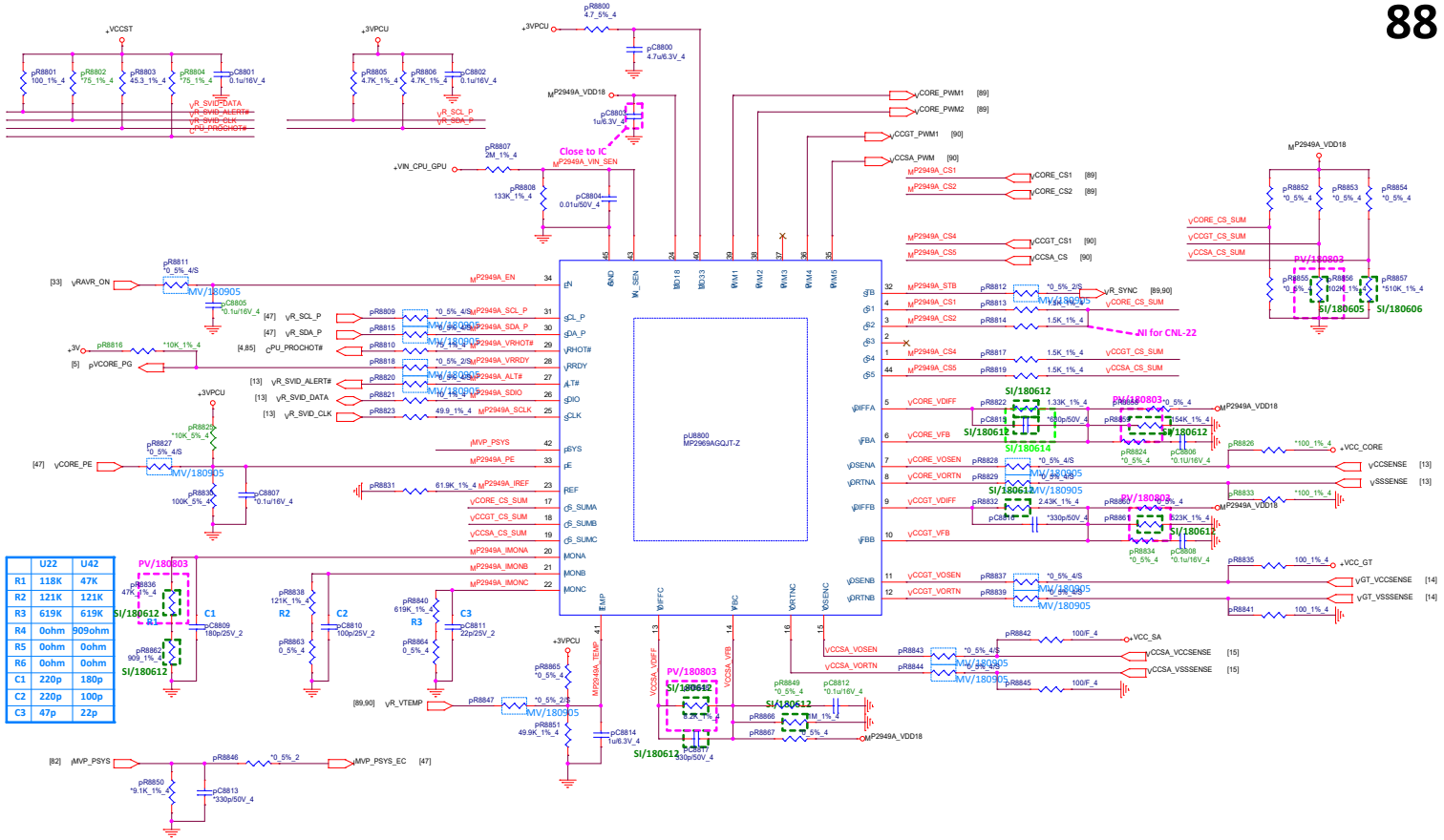
Size	Document Number	Rev
Custom	85 – Charger II	1 A
Date: Monday, October 29, 2018	Sheet 85 of 106	



[5,7,12,33,34,36,41,42,47,48,50,54,58,61,73,75,77,80,81,82,85,87,88,92,93,95] +3VPCU
[81,63,73,76,80,81,87,89,90,92,95,96] +5VPCU
[73,81,82,87,93,97] +VIN

NB5	PROJECT : G7B Quanta Computer Inc.		
Size: Custom	Document Number: 6 – +3/5VS(SY8286B/SY8286C)		Rev: 1A
Date: Monday, October 29, 2018	Sheet: 86	of: 106	

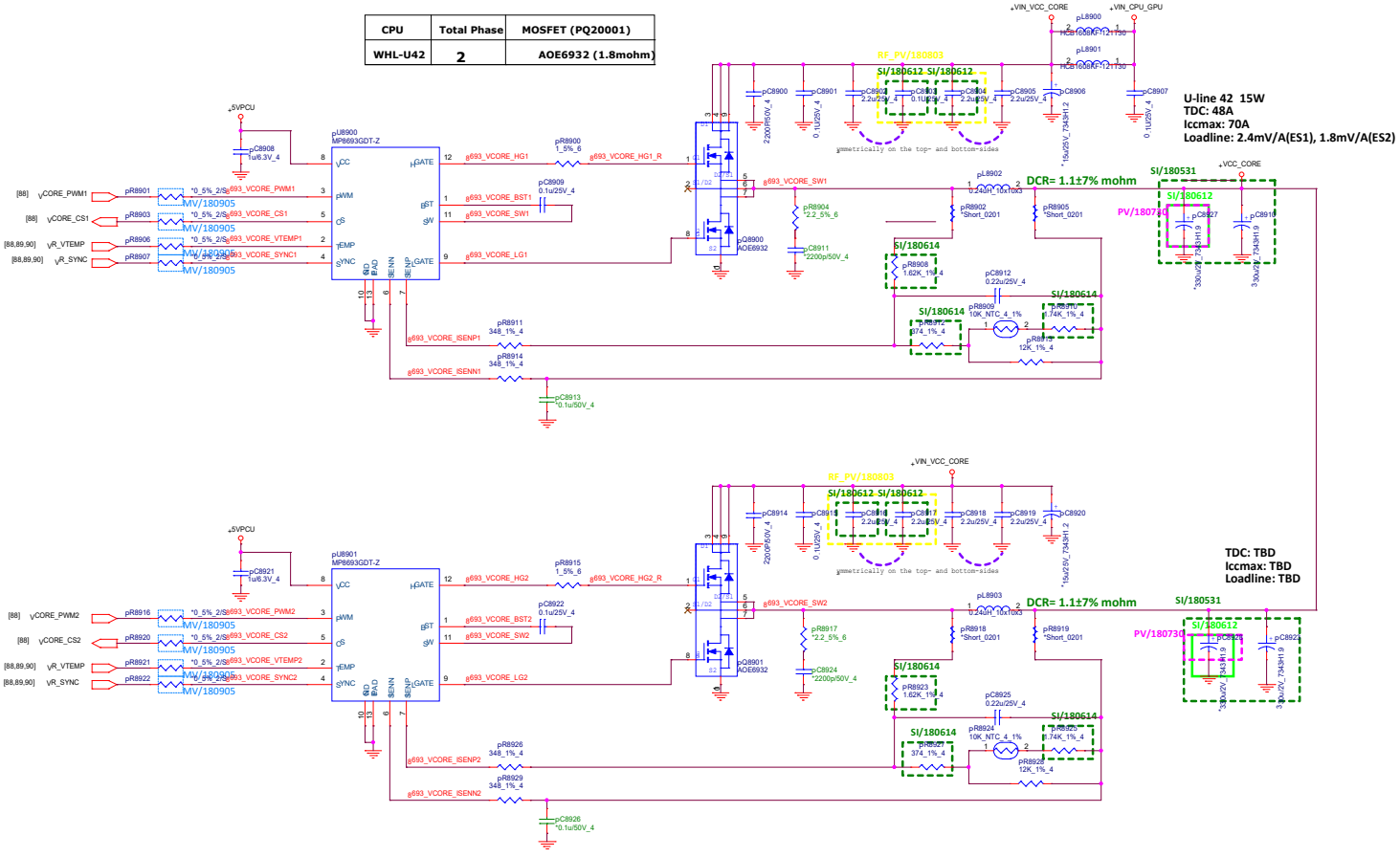

+1.2VSUS +/-5%
Continue current: 6A
Peak current: 10A
OCP (min.): 12A
0.6A (max.)
10mA (max.)
DCR= 10 mohm (max.)
SI/180612 SI/180612
SI/180531
symmetrically on the top- and bottom-sides
+2.5VSUS +/-5%
Continue current: 1A
Peak current: 1.1A
DCR= 43 mohm (max.)
VFB= 0.6V
RT8231BGQW
RT8097ALGE
VID | Reference Voltage (V)
High | 0.675
Low | 0.75
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PROJECT :X8B
Quanta Computer Inc.
Document Number
87 -- DDR4 (RT8231B)
Monday, October 29, 2018
Sheet 87 of 106

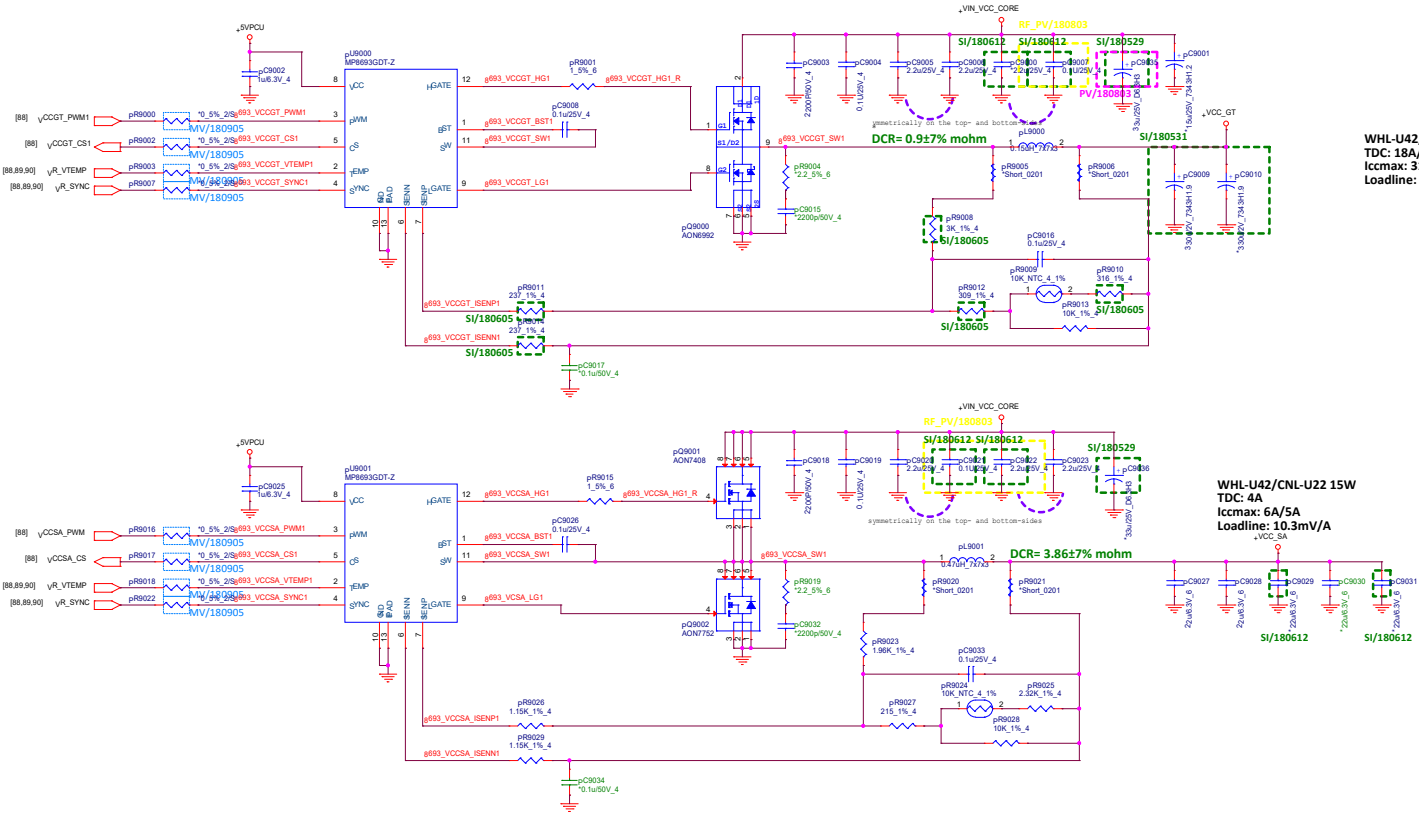


	U22	U42
R1	118K	47K
R2	121K	121K
R3	619K	619K
R4	0ohm	909ohm
R5	0ohm	0ohm
R6	0ohm	0ohm
C1	220p	180p
C2	220p	100p
C3	47p	22p

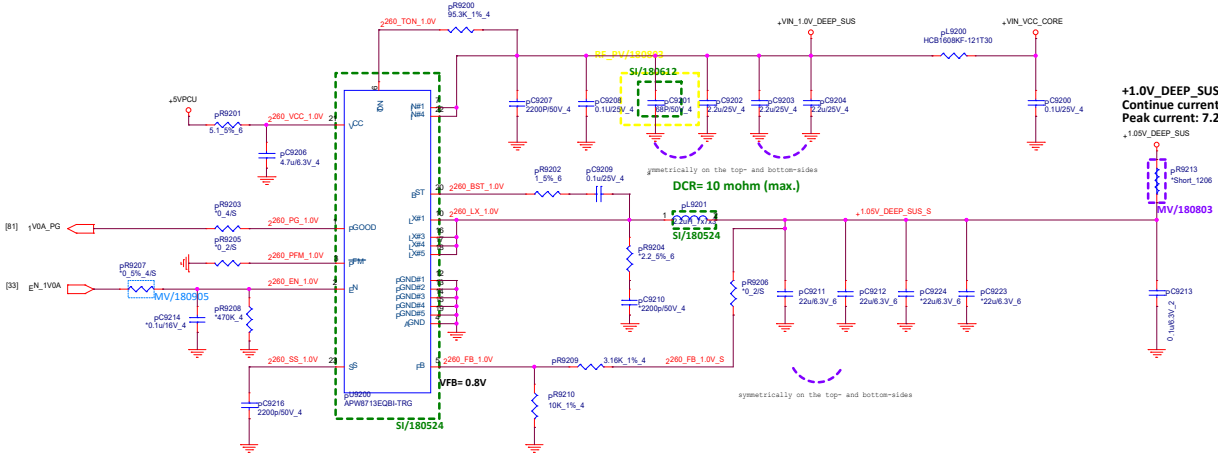
NB5	PROJECT : Megatron Quanta Computer Inc.	
Size: Custom	Document Number: 8g – CPU CORE VR (MP2949A)	Rev: 1A
Date: Monday, October 29, 2018	Sheet: 88 of 97	

CPU	Total Phase	MOSFET (PQ20001)
WHL-U42	2	AOE6932 (1.8mohm)

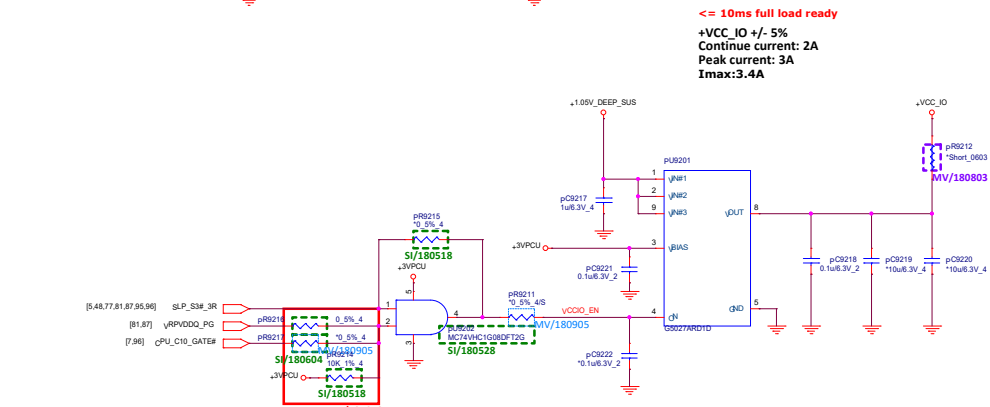


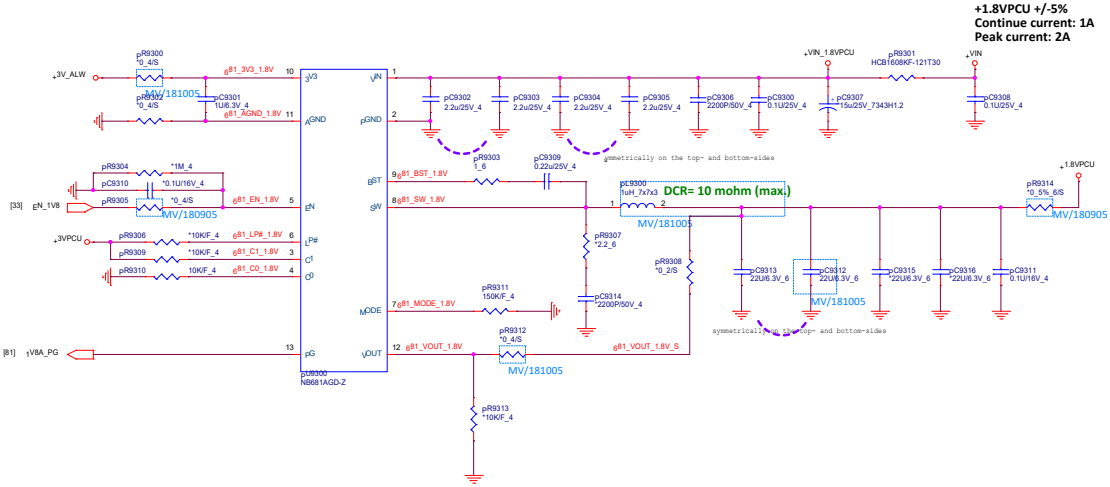


NB5	PROJECT : Megatron Quanta Computer Inc.			
	Size: Customs	Document Number: 90 -- +VCC_GT/+VCC_SA		Rev: 1A
	Date: Monday, October 29, 2018	Sheet: 90 of 106		



V_o	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



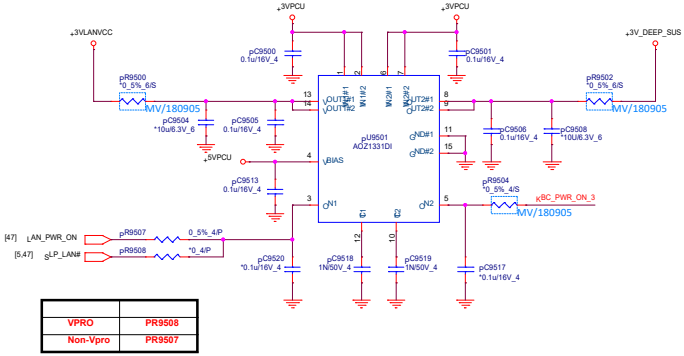


MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

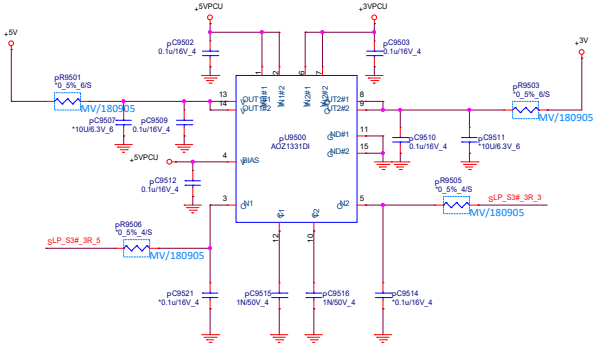
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

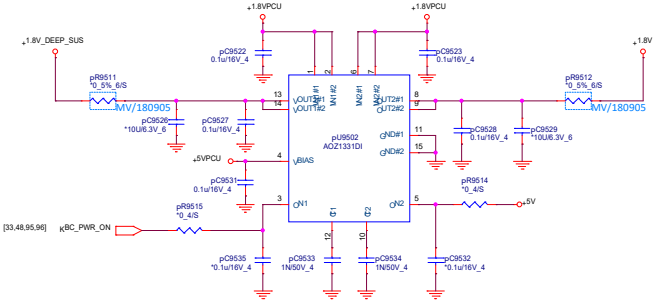
Note: LP#, CO and C1 are pulled high internally

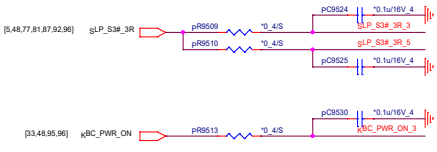
QUANTA COMPUTER CONFIDENTIAL

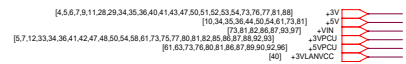


VPRO	PR9508
Non-Vpro	PR9507



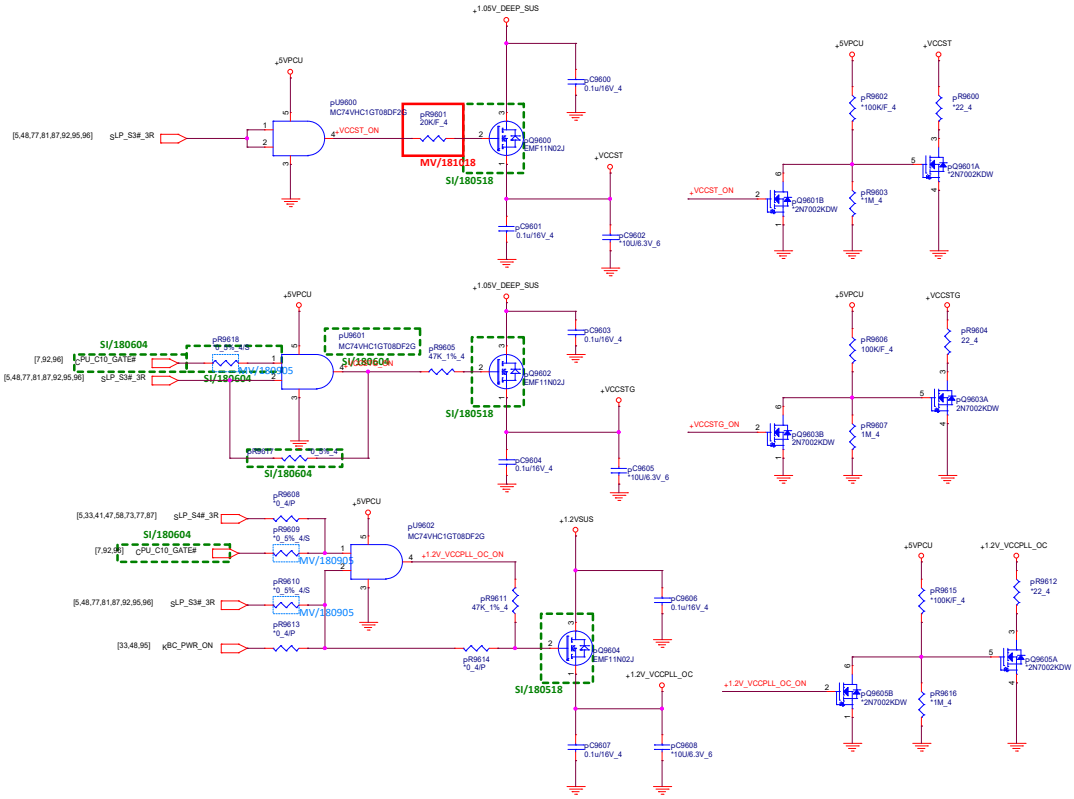






PROJECT :X8B
Quanta Computer Inc.

Size: Custom	Document Number: 9S – Load Switch I (AOZ1331DI)	Rev: 1A
Date: Monday, October 29, 2018	Sheet: 95 of 106	

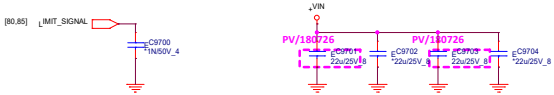


[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95] +3V
[10,34,35,36,44,50,54,61,73,81,95] +5V
[73,81,82,86,87,93,97] +VIN
[5,7,12,33,34,36,41,42,47,48,50,54,58,61,73,75,77,80,81,82,85,86,87,88,92,93,95] +3VPCU
[61,63,73,76,80,81,86,87,89,90,92,95] +5VPCU
[40,95] +3VLANVCC

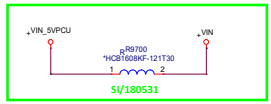
PROJECT :X8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	9G – Load Switch II	1A
Date: Monday, October 29, 2018	Sheet 96 of 106	

Reserve for EMI & ISEN test



RF Cap



PROJECT :X8B Quanta Computer Inc.		
Size: Custom	Document Number: 97 – ISN and EMI CAP	Rev: 1A
Date: Monday, October 29, 2018	Sheet: 97 of 106	